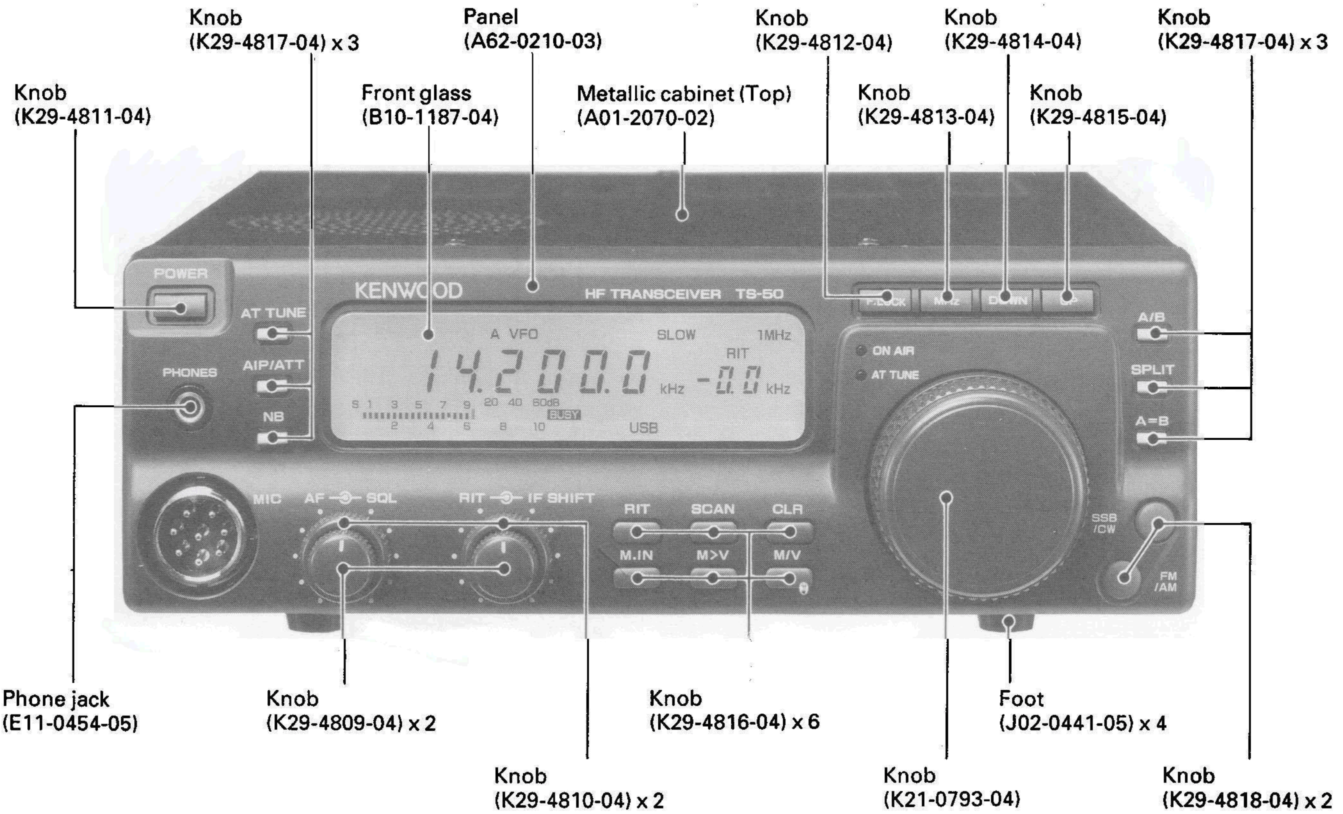
HF TRANSCEIVER

TS-50S

SERVICE MANUAL

KENWOOD

B51-8199-00 (O) 1676



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CIRCUIT DESCRIPTION

Frequency Configuration

The TS-50S uses double conversion in all transmission modes, double conversion in all reception modes except FM, and triple conversion in FM reception mode. (Fig. 1)

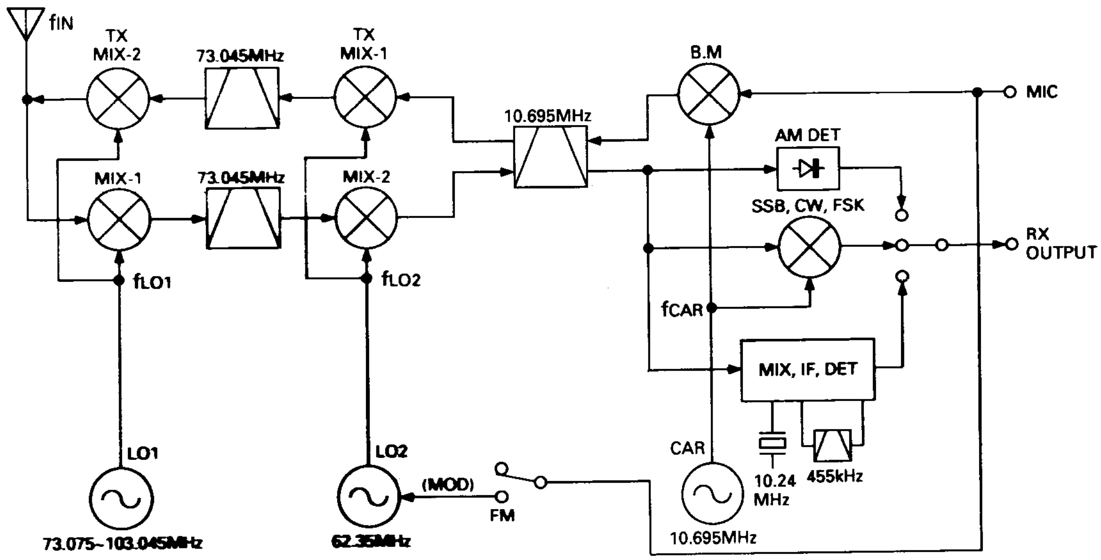


Fig. 1 Frequency configuration

The receiver frequency in SSB mode is given by the following equation when the receiver tone produced by the input frequency (f_{IN}) from the antenna is zero beat (when an SSB signal with a carrier point of fin is zeroed in):

$$f_{IN} = f_{LO1} - f_{LO2} - f_{CAR}$$

Since all these frequencies are generated by the PLL circuit, as shown in Figure 2 (PLL frequency configuration), the receiver frequency is determined only by the reference frequency, f_{STD}, and the PLL divide ratio. This means, the accuracy of the reference frequency determines the accuracy of the operating frequency of the transceiver.

The accuracy of the reference crystal oscillator used in the TS-50S is 10 ppm (–10 to +50°C). The accuracy of the optional temperature-compensated crystal oscillator (TCXO, SO-2) is 0.5 ppm (–10 to +50°C).

In SSB transmission mode or in other modes, the frequency is determined by the reference frequency (f_{STD}) and the PLL divide ratio. Table 1 lists the display frequencies in the various modes.

The pitch of the incoming signal in CW mode can be varied in 50-Hz steps in the range 400 to 1000Hz without changing the center frequency of the IF filter (variable CW pitch system).

FM transmission is carried out by applying the audio signal from the microphone to the 62.35-MHz VCO and modulating f_{LO2}.

Mode	Display frequency
USB, LSB	Carrier point frequency
CW	Transmit carrier frequency
AM, FM	IF filter center frequency

Table 1 Display frequency in each mode

PLL Circuit Configuration

The TS-50 PLL circuit uses a reference frequency of 20MHz, and covers 30kHz to 30MHz in 5- to 200-Hz steps, depending on how fast the encoder is turned. Figure 2 shows the frequency configuration of the PLL circuit. Figure 3 is a PLL block diagram.

1. Reference oscillator circuit

The reference frequency (f_{STD}) for frequency control is generated by the 20-MHz crystal oscillator, X1 and Q12 (2SC2714(Y)). The reference frequencies for other circuits are produced by dividing f_{STD} by two and by five by IC2 (µPD74HC390G). f_{STD} is divided by two to produce a 10-MHz PLL reference signal, which goes to IC11 (CXD1225M) and IC101 (CXD1225M). It is input to the CAR oscillator section to produce a 10.695-MHz signal. The 4-MHz signal produced by dividing f_{STD} by five goes to IC4 (SN16913P).

The crystal oscillator circuit can be replaced by an optional TCXO (SO-2). The TS-50S can be switched to the TCXO by removing a shorting jumper (W1/W2).

CIRCUIT DESCRIPTION

2. LO2 (PLL loop)

The VCO of IC10 (KCH14) generates a signal of 62.35MHz. The 10-MHz reference frequency is applied to pin 5 of IC101 (CXD1225M), and is divided by 200 (800 in FM mode) to produce a 50-kHz (12.5-kHz in FM mode) comparison frequency. The output from the VCO is applied to pin 11 of IC101, and is divided by 1247 (4988 in FM mode). It is then compared with the 50-kHz (12.5-kHz in FM mode) reference signal by the phase comparator to lock the VCO frequency. Divide ratio data is supplied by the digital unit.

The output is amplified by amplifier Q18 (2SC2954) and passes through a low-pass filter. The VCO is modulated in FM mode.

3. LO1 (PLL loop)

Q1 to Q3 (2SK508NV) in the X58-4010-00 are VCOs. Q1 generates a signal of 73.075 to 83.544MHz; Q2, a signal of 83.545 to 94.544MHz; and Q3, a signal of 94.545 to 103.045MHz. The 10-MHz reference signal is input to pin 5 of IC11 (CXD1225M) and is divided by 20 to produce a 500-kHz comparison frequency. The output signal from the VCO is mixed with a 55.045- to 55.545-MHz signal from the PLL (described later) to produce a 18.5- to 47.5-MHz signal. It is input to pin 11 of IC11, divided, and compared with the 500-kHz signal by the phase comparator, and the VCO frequency is locked. Divide ratio data is supplied by the digital unit.

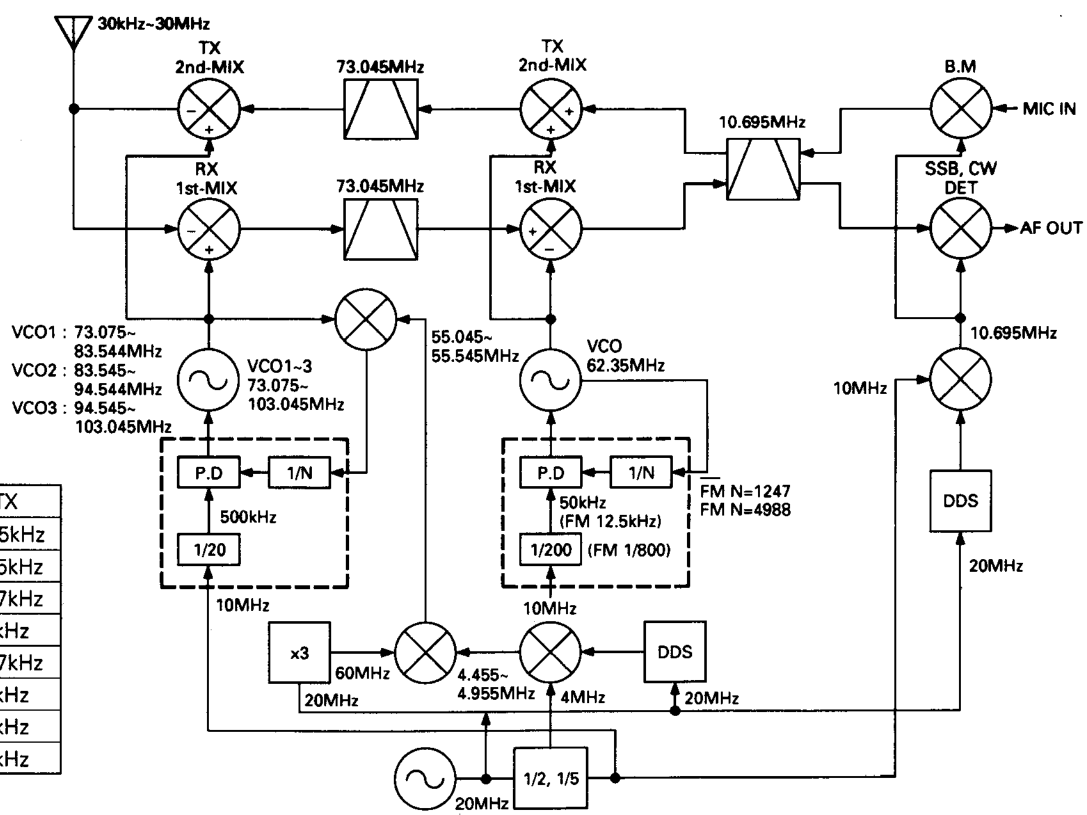
The 20-MHz reference signal is input to DDS1 (X58-4020-00), and the output signal is mixed with a 4-MHz signal by IC4 to generate a signal of 4.455 to 4.955MHz (in 5- or 200-Hz steps). The signal is mixed with the 60-MHz signal (3 x 20-MHz reference frequency) by IC5 (SN16913P) to produce a 55.045 to 55.545MHz signal (in 5- or 200-Hz steps).

4. CAR

The 20-MHz reference signal is input to DDS2 (X58-4020-00), and the output signal is mixed by IC7 (SN 16913P) with the 10MHz signal divided by IC2 to produce a 10.695-MHz signal. This signal passes through the band-pass filter and amplifier and is output for local oscillation and detection.

5. DDS

The DDS is the same as that used in the TS-950.



	RX	TX
USB	+1.5kHz	+1.5kHz
LSB	−1.5kHz	−1.5kHz
CW W	+1.5kHz	−0.7kHz
CW N	+0.8kHz	0kHz
CW RW	−1.5kHz	−0.7kHz
CW RN	−0.8kHz	0kHz
AM	−	0kHz
FM	−	0kHz

Fig. 2 PLL circuit frequency configuration

CIRCUIT DESCRIPTION

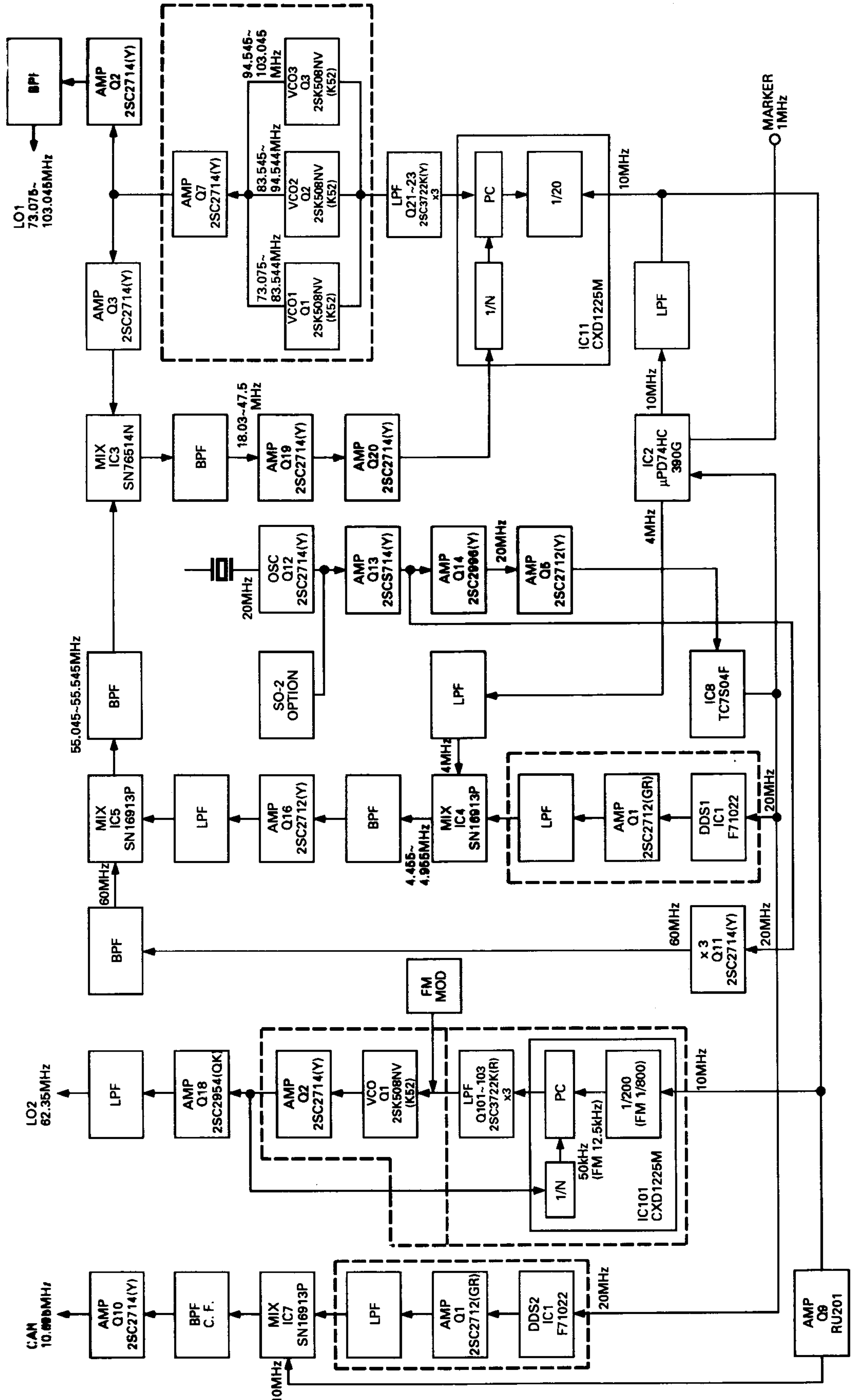


Fig. 3 PLL block diagram

CIRCUIT DESCRIPTION

Receiver Circuit Configuration

The configuration of the receiver circuit is double-conversion with a first IF of 73.045MHz and a second IF of 10.695 MHz, and triple-conversion in FM mode with a first IF of 73.045MHz, a second IF of 10.695MHz, and a third IF of 455kHz. (Fig. 5)

The incoming signal from the antenna passes through the antenna switch relay on the filter unit, then through the 30-MHz low-pass filter, and goes to the TX-RX unit. The signal passes through a 20dB attenuator and 30-MHz low-pass filter in the TX-RX unit, and goes through the eight band-pass filters. If AIP is off, the signal passing through each band-pass filter is amplified by the RF amplifier, Q9 and Q10 (2SK520 x 2), and is input to the first mixer, Q5 to Q8 (2SK520 x 4). If AIP is on, the signal bypasses Q9 and Q10 and goes directly to the first mixer. It is mixed with the LO1 signal by the first mixer to produce a first IF signal of 73.045MHz.

The first IF signal of 73.045MHz passes through the MCF (XF1), is amplified by Q17 (3SK131), and mixed with the 62.35-MHz LO2 signal by the second mixer, Q18 and Q19 (2SK520 x 2), to produce a second IF signal of 10.695MHz.

The second IF signal of 10.695MHz is split into two. One signal goes to the NB amplifier, and the other passes through the NB gate FET (3SK131). The signal then passes through the CF (XF2) and is detected by IC2 (KCD04) in FM mode. In other modes, the signal goes to the IF filter of the X48-3110-00 unit. There are three types of IF filter: 6-kHz, 2.7-kHz, and 500-Hz (500-Hz is optional). The signal passing through the IF filter goes to IC3 (KCD08), and is product-detected in SSB and CW modes, and envelope-detected in AM mode.

1. Receiver front-end

The signal input to the TX-RX unit passes through the switching circuit of the attenuator and the 30-MHz low-pass filter, and goes to seven band-pass filters. If AIP is off, D10 and D11 turn on and D8 and D9 turn off, and the signal passing through each filter is amplified by about 13 dB by Q9 and Q10 (2SK520 x 2) and output to the first mixer. If AIP is on, D10 and D11 turn off and D8 and D9 turn on, and the signal is output directly to the first mixer without passing through Q9 and Q10. The first mixer, is a quad balanced mixer, Q5 to Q8 (2SK520 x 4). (Fig. 4)

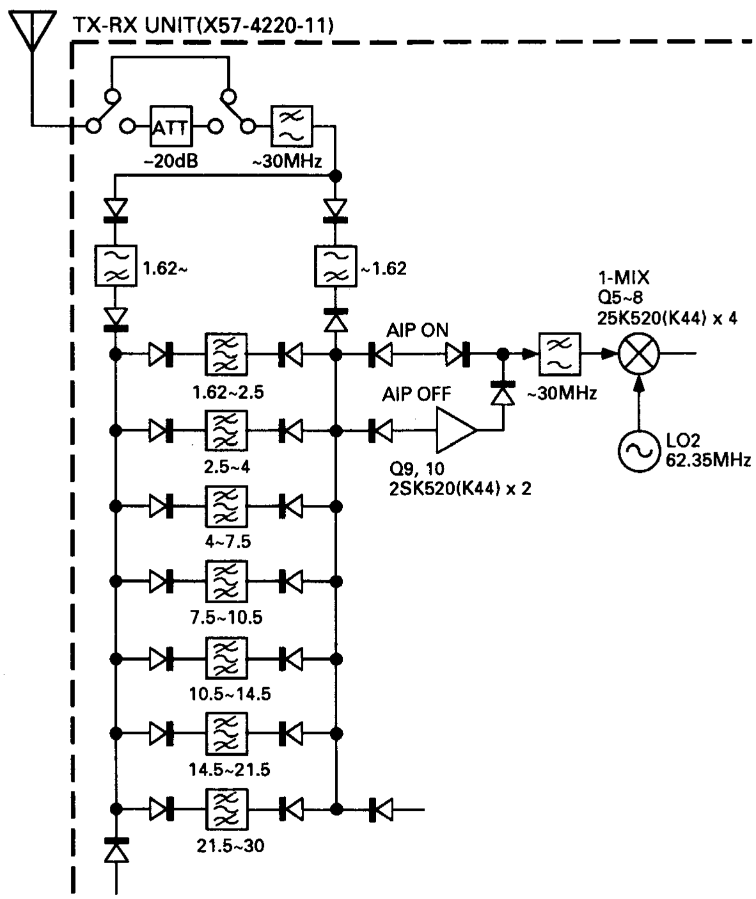


Fig. 4 Receiver front-end

CIRCUIT DESCRIPTION

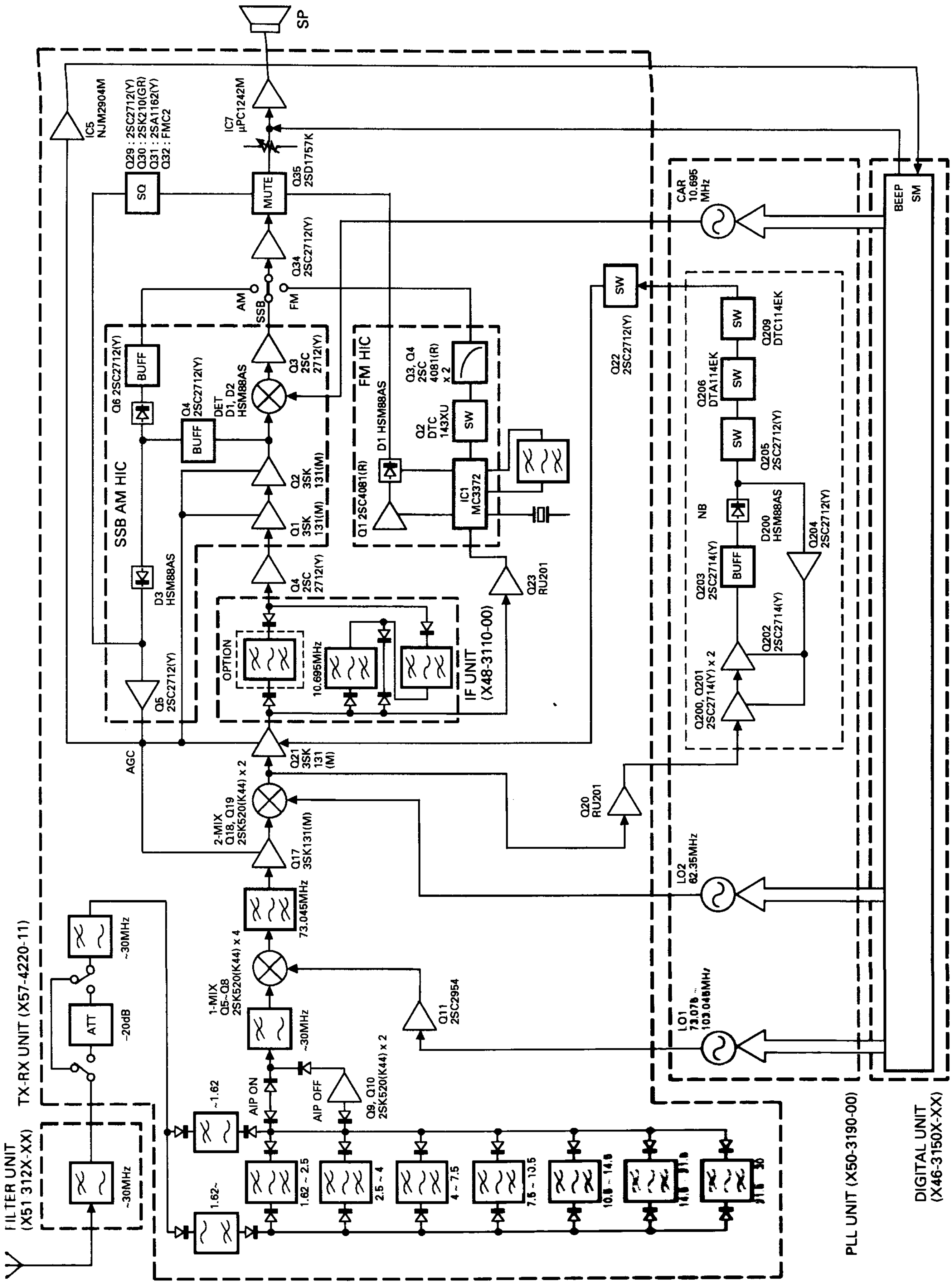


Fig. 5 Receiver section bock diagram

CIRCUIT DESCRIPTION

2. Noise blanker circuits

The 10.695-MHz IF signal generated from the first IF of 73.045MHz by the second mixer is input to IF amplifier Q21 (3SK131), sent through Q20, amplified by noise amplifier Q200, Q201, and Q202 (2SC2714), sent through buffer Q203, and noise-detected by D200. This signal switches Q205, Q206, and Q209, and controls Q22 in the TX-RX unit. Q22 controls IF amplifier Q21 and blanks the noise.

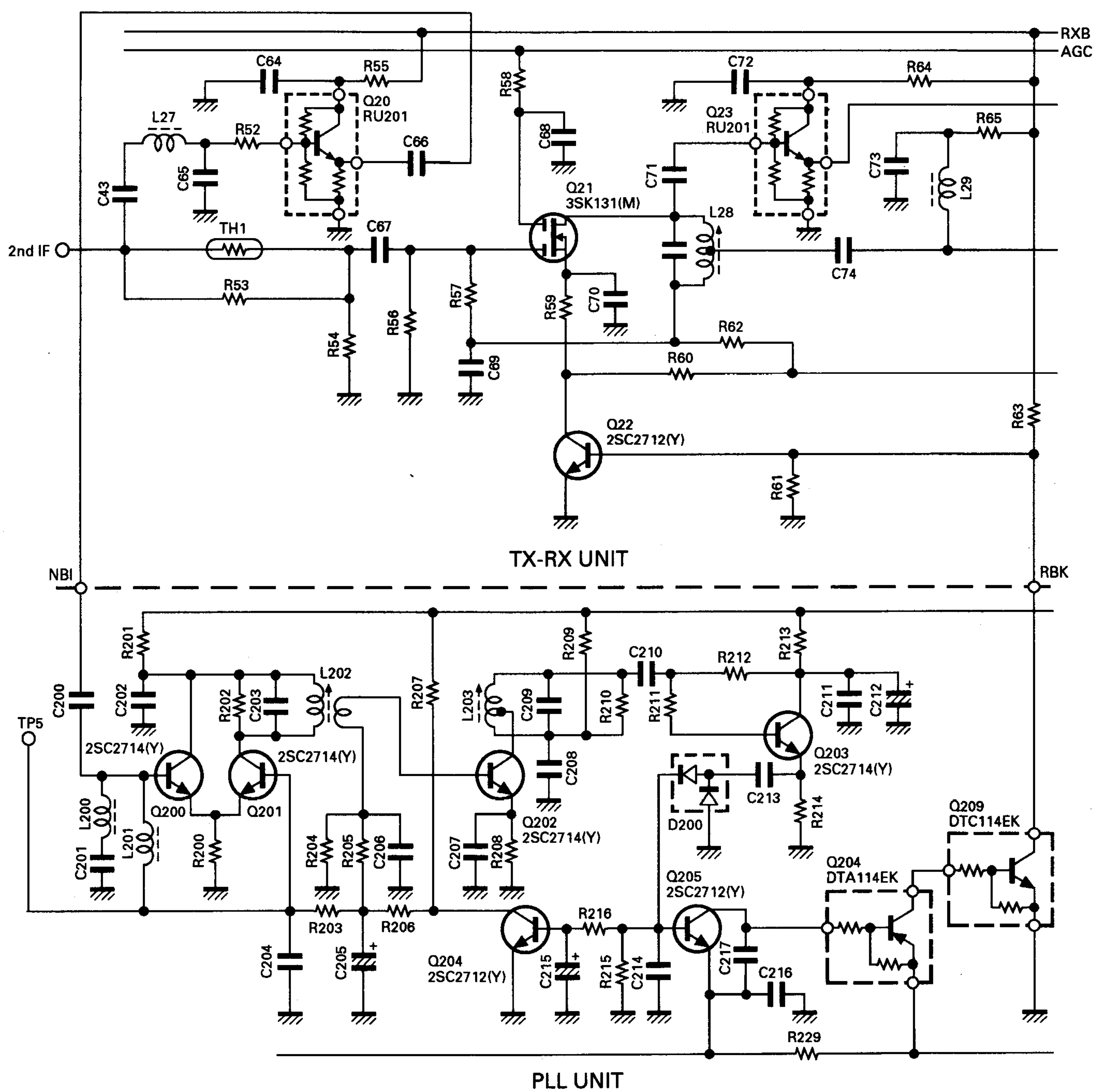


Fig. 6 Noise blanker circuits

CIRCUIT DESCRIPTION

3. SSB, AM, CW filter circuit

The second IF signal amplified by Q21 is input to the X48-3110-00 unit in all modes except FM.

If an optional CW filter (XF1) is installed and CW NARROW is elected in CW mode, the signal passes through XF1 according to the control signal from the microcomputer. If XF1 is not installed or CW NARROW is not selected, the signal passes through XF3 and XF2.

In SSB mode, the signal passes through XF3 and XF2.

In AM mode, the signal passes through XF3 and XF2 as in SSB mode if AM NARROW is selected. If AM NARROW is not selected, the signal passes through XF2 only.

In FM mode, the signal does not pass through the filter circuit in this unit.

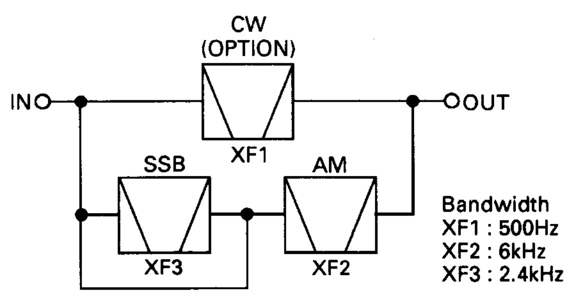


Fig. 7 Filter circuit

Item	Rating
Nominal center frequency	10,695kHz
Center frequency deviation	Within ±80Hz at 6dB
Pass bandwidth	500Hz or more at 6dB
Insertion loss	Within 5dB ± 2dB
Terminating impedance	1200Ω/6pF

Table 2 MCF (L71-0283-05) : IF unit XF1 (Option)

Item	Rating
Nominal center frequency	10.695MHz
Pass bandwidth	6kHz or more at 6dB
Attenuation bandwidth	40kHz or less at 60dB
Ripple	2dB or less
Insertion loss	3dB or less
Guaranteed attenuation	60dB or more within fo ± 1MHz
Terminating impedance	1.2kΩ ± 10% / 6pF ± 10%

Table 3 MCF (L71-0433-05) : IF unit XF2

Item	Rating
Nominal center frequency	10.695MHz
Center frequency deviation	Within ±200Hz at 6dB
Pass bandwidth and Attenuation bandwidth	2.2kHz or more at 6dB
	±1.5kHz or less at 20dB
	±2.4kHz or less at 60dB
Ripple	2dB or less
Insertion loss	5dB or less
Guaranteed attenuation	60dB or more within fo ± 40kHz
Terminating impedance	1.2kΩ ± 5% / 6pF ± 5%

Table 4 MCF (L71-0249-05) : IF unit XF3

4. SSB, AM, CW detection circuit

After unwanted signal components have been removed in the X48-3110-00 unit, the signal is input to IC3 (KCD08). The signal amplified by IC3 is mixed with the CAR signal input from CN11 in SSB and CW modes, and detected to output an audio signal. In AM mode, the signal is envelope-detected by the diode and capacitor to output an audio signal.

5. FM detection circuit

The impedance of the second IF signal amplified by Q21 is converted by Q23 (RU201) in FM mode, and unwanted signal components are removed by the CF (XF2). The resulting signal is input to the detection IC (IC2: KCD04). The signal is then mixed with the 10.24-MHz oscillator signal to generate the 455-kHz signal. The signal is passed through ceramic filter CF1, and detected by the quadrature detector with the signal phase-shifted by CD1.

6. Squelch circuit

In all modes except FM, the 10.695-MHz IF signal is detected by a diode in IC3, passed through Q29 and Q30, and a voltage proportional to the signal level appears at the base of Q31. When the SQ VR is turned clockwise, the emitter voltage of Q31 increases and Q32 is switched on.

In FM mode, as the IF signal increases, the noise level decreases, and the voltage at the SQ pin decreases, making the SC pin low. When the SQ VR is turned clockwise, the voltage at the SQ pin rises, and the SC pin goes high. Current flows through R77, and Q32 turns on.

Q35 turns on to mute the AF signal line. (Fig. 8)

CIRCUIT DESCRIPTION

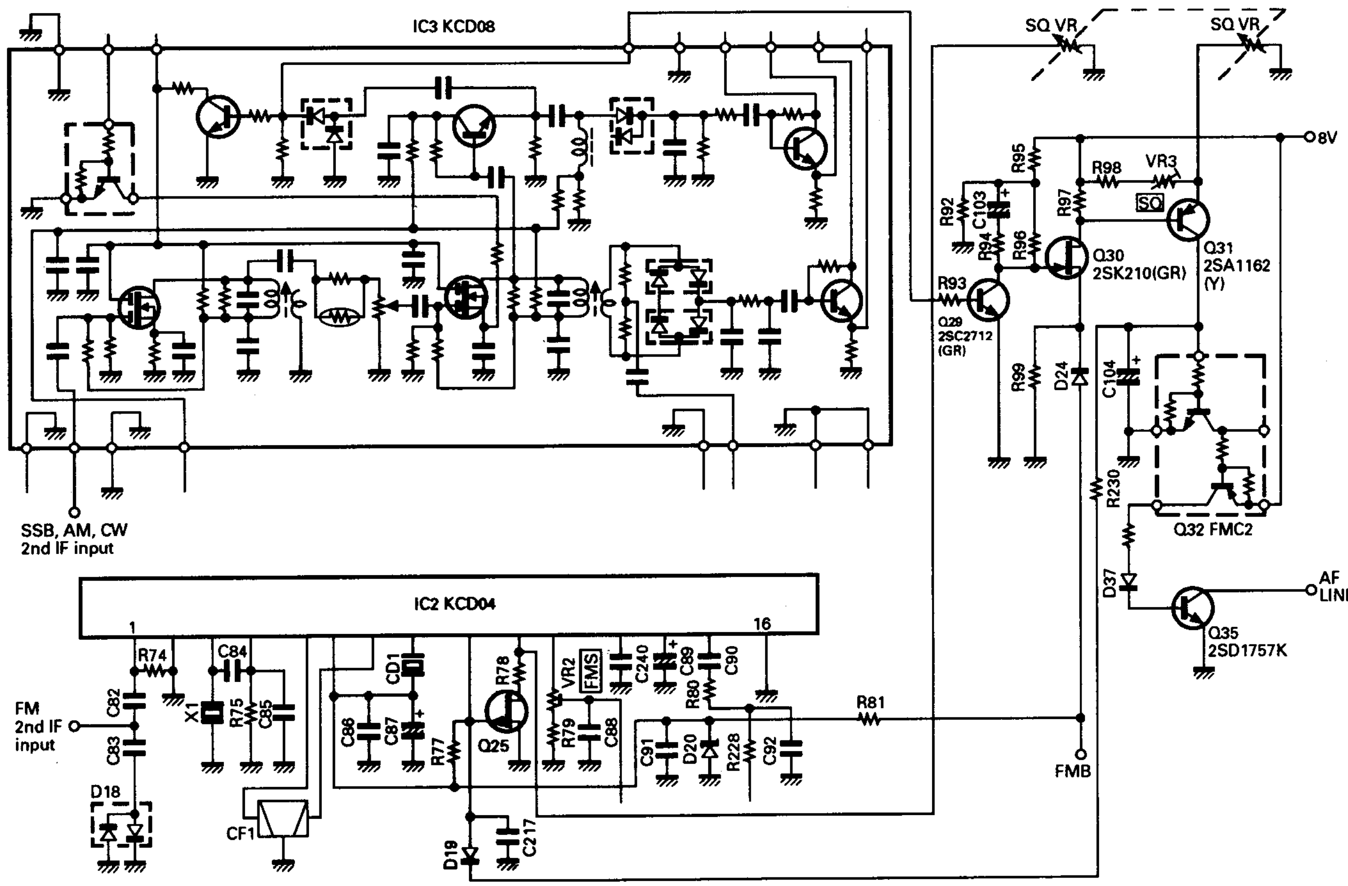


Fig. 8 Squelch circuit

7. Signalstrength meter circuit

In all modes except FM, the signalstrength meter circuit comprises operational amplifier IC5. The signal, level-detected by IC3, is input to IC5 (1/2) and amplified by about 8 dB by IC5 (2/2).

In FM mode, the level detection signal from IC2 is adjusted by VR2, selected by IC4 (BU4066BF) according to the mode, and output directly to the digital unit. (Fig. 9)

8. AGC circuit

The time constant for the signal envelope-detected by IC3 is changed in each mode by the analog switch. The effective value, not the peak value, is used in AM mode. When SLOW is selected in SSB and CW modes, the analog switch is turned on. (Fig. 9)

CIRCUIT DESCRIPTION

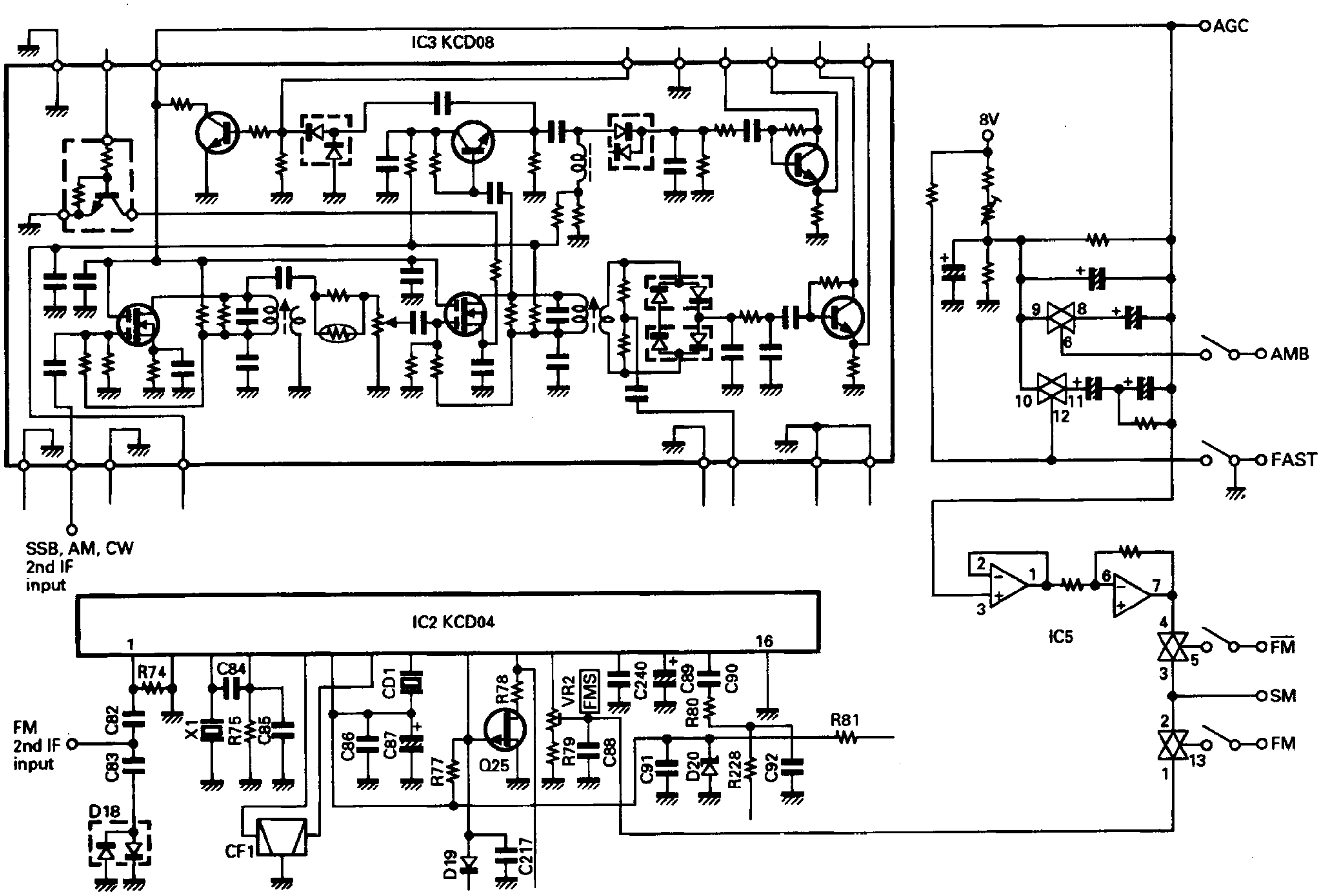


Fig. 9 S-meter and AGC circuits

Transmitter Circuit Configuration

The audio signal from the microphone enters CN15 of the TX-RX unit. The signal then goes to Q38 (2SC3722K) of the microphone amplifier, and is split and directed to the SSB and FM systems. In the SSB system, the signal, its gain properly adjusted by VR7, is amplified by Q40 (2SC2712(Y)), balance-modulated with the CAR signal (10.695MHz) input from CN11 by IC8 (μPC1037HA), passed through Q42 (2SC2712(Y)), and sent to the crystal filter in the X48-3110-00 unit. The SSB signal passing through the filter is amplified by Q43 (3SK131M).

The 62.35-MHz LO2 signal from the PLL unit is input from CN3 of the TX-RX unit, and mixed with the 10.695-MHz signal amplified by Q43, Q46, and Q47 (3SK131(M)) to produce a 73.045-MHz signal. The LO1 signal from the PLL unit is input from CN2 of the TX-RX unit, and mixed with the 73.045-MHz signal by Q48 and Q49 (3SK131(M)) to generate the desired signal. The signal passes through the band-pass filter and is amplified by Q50 (2SC2954) to produce the drive output, which goes to the final unit from CN19.

The signal is amplified to the appropriate power level for the type by the final unit. Harmonic components are attenuated by the filter unit, and the signal is output from the antenna connector.

In FM mode, the audio signal amplified by microphone amplifier Q38 and Q39 is input to CN1 of the PLL unit, and passes through the pre-emphasis and IDC circuit of IC201 to modulate LO2 (62.35MHz).

In AM mode, the signal is generated by unbalancing the carrier of SSB balance modulator IC8.

In CW mode, Q59 of the TX-RX unit is switched by the key, and the signal is input to IC1 of the digital unit. The sidetone monitor signal is generated by X59-4000-00 in the TX-RX unit, and output from the speaker. The CW control signal is output from IC1 of the digital unit, and input from CN17 of the TX-RX unit to switch Q46 and Q47 and generate the CW signal. (Fig. 10)

CIRCUIT DESCRIPTION

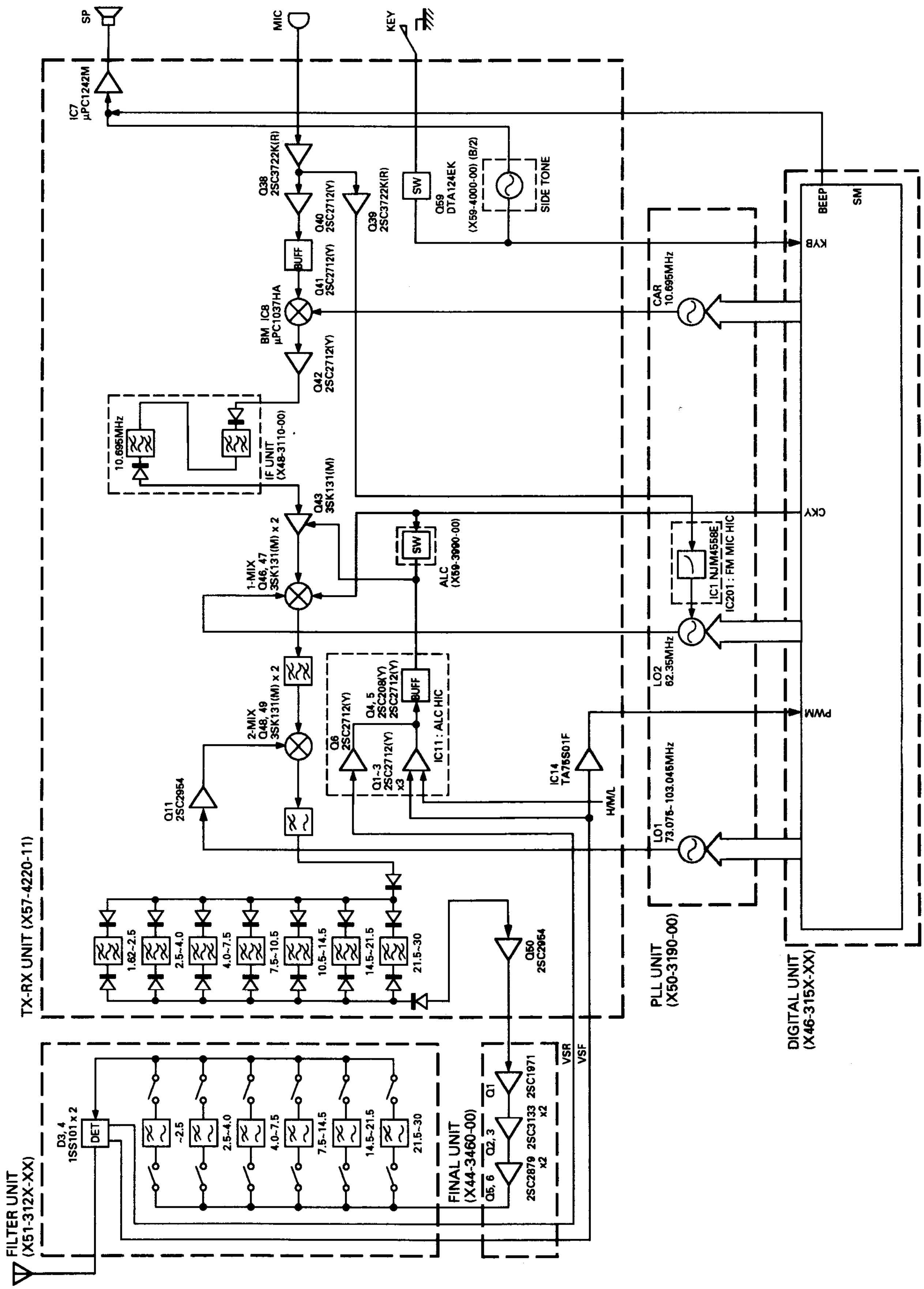


Fig. 10 Transmitter section block diagram

CIRCUIT DESCRIPTION

1. ALC circuit

The forward wave voltage detected in the filter unit passes through CN18 in the TX-RX unit, its level is adjusted by VR14, and it is applied to the differential amplifier comprising Q1 and Q2 (2SC2712(Y) x 2) in IC11. When VSF is applied to the base of Q1, the emitter voltage of Q1 and Q2 increases and the current flowing through the base of Q2 decreases; thus the collector voltage rises. When this voltage exceeds the emitter voltage of Q3 (2SC2712(Y)) (about 1.8V) plus VBE (about 0.6V), the current flows through the base of Q3 and the collector voltage drops. ALC time constants C and R are connected to this collector.

The collector voltage change is shifted by Q4 (2SK208) and D2 (3.6V), and matched with the voltage for keying by Q5 and D3 (RLS73) to generate the ALC voltage. This ALC voltage activates ALC by lowering the second gate voltage of Q43 (3SK131(M)) of the TX-RX unit. (Fig. 11)

2. Power control circuit

Power is controlled by lowering the base voltage of Q2 in IC11. As the base voltage of Q2 decreases, the emitter voltage of Q1 and Q2 decreases. This activates ALC and reduces the power even if the base voltage (VSF) of Q1 is low. The power is changed by IC12. In AM mode, Q63 turns on, and the power is reduced to about 1/4 of the power in other modes. (Fig. 11)

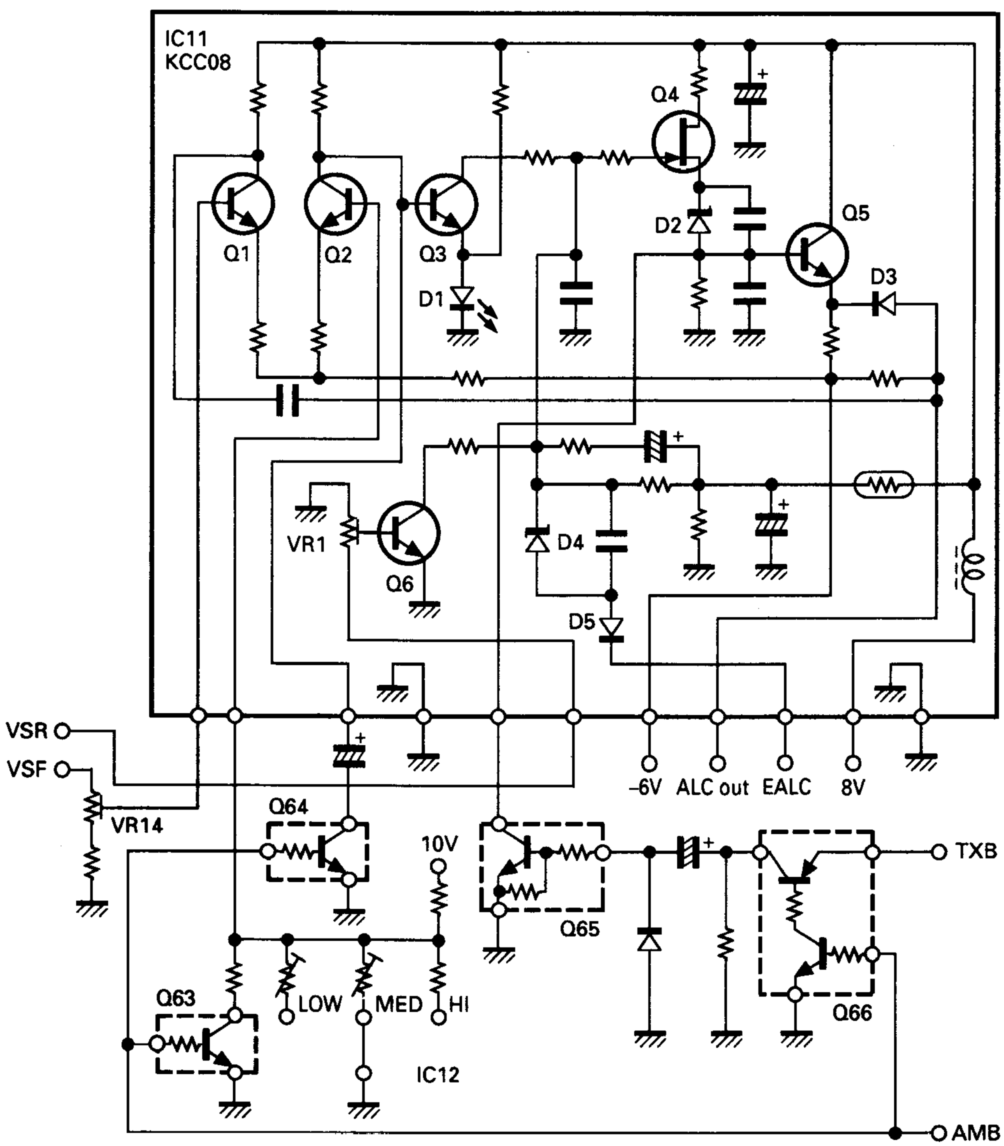


Fig. 11 ALC and power control circuits

CIRCUIT DESCRIPTION

3. Protection circuit

When the reflected wave voltage (VSR) detected by the filter unit rises, Q6 (2SC2714(Y)) in IC11 turns on to reduce the voltage of the ALC time constant line. The drive is decreased and the power is reduced to protect the final transistor.

4. Temperature protection

If the final heat sink temperature rises, Q8 in the final unit turns on and the fan starts running at low speed in both transmit and receive modes. If the final heat sink temperature rises further, Q9 turns on, and the fan rotates at medium speed in both transmit and receive modes. If the temperature rises further still, the fan rotates at high speed in transmit mode, and at medium speed in receive mode to reduce the fan noise.

If the temperature continues to rise, the temperature detection port of the microcomputer (IC1 in the digital unit) is made high to reduce the RF output forcibly. If the fan fails or does not rotate because something is stopping it, the RF output is forcibly reduced in the same way.

Digital Control Circuit

The TS-50S digital control circuit comprises a 16-bit microcomputer (M37702M4A-FP), a reset IC (M62003FP), an EEPROM (NM93C66EM8), a latch (TC74HC573AF), and a decoder (TC74HC238AF). The latch and decoder are used to expand the output ports. The decoder outputs an enable signal pulse.

Since there are many control signals for the TX-RX unit and filter unit, they are output to the shift register (serial-to-parallel converter) in series. (Fig. 13)

1. Power button

With this transceive, the power is turned on and off by the microcomputer. When the power button is pressed, the microcomputer detects it and energizes, the power relay to supply 14V to the transceiver. When the power button is pressed to turn the transceiver off, the microcomputer checks it a little longer than when turning the power on, and deenergizes the power relay.

2. Reset circuit

IC4 (M62003FP) monitors Vcc applied to the microcomputer. If the voltage falls below 2.15V, the IC outputs a reset signal (low) to the microcomputer, and the CPU initializes all internal data (including memory channel data). The reset signal is not output when the power is turned on or off or 14V is turned on or off. It is output when the battery voltage level goes low and 14V is turned on or off.

C35 generates the signal width (td) required to reset the microcomputer. (Fig. 12)

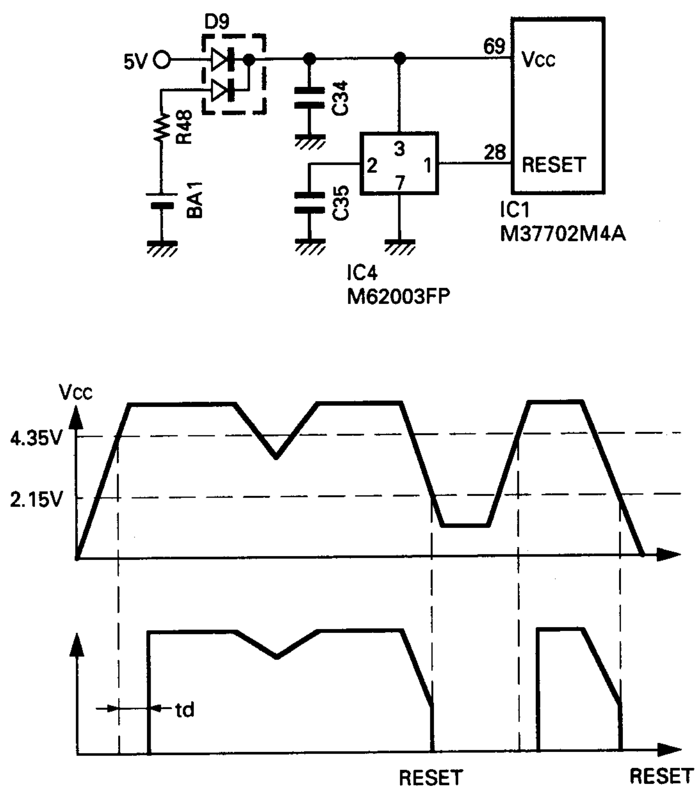


Fig. 12 Reset circuit

CIRCUIT DESCRIPTION

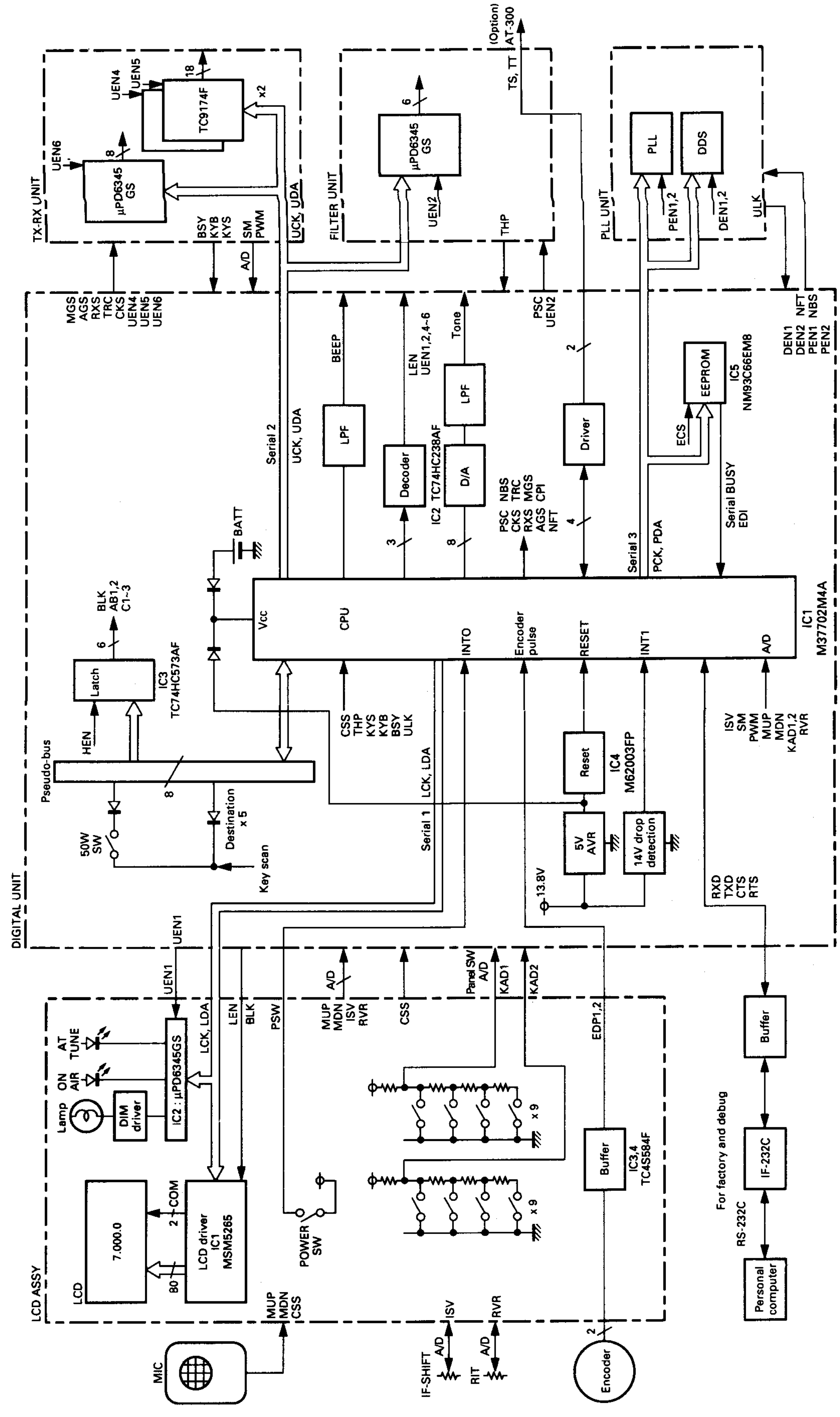


Fig. 13 Digital control block diagram

CIRCUIT DESCRIPTION

3. Backup circuit

This transceiver has two kinds of data stored in the microcomputer and EEPROM. User data, such as memory channel data, is stored in the microcomputer, and adjustment data, such as meter curves, is stored in the EEPROM. The EEPROM data is retained when the power supply voltage is off, but power is required to retain the microcomputer data. If 14V is not cut off, power is supplied from the 5V AVR in the digital unit. If 14 V is cut off, power is supplied from a lithium battery. To retain data with the lithium battery, the microcomputer must be in backup mode. So, the backup circuit shown in Figure.14 detects a voltage drop in the 14V line and outputs a backup request signal to the microcomputer.

4. PLL and DDS control circuit

The TS-50S has three PLLs and two DDSs. The main microcomputer outputs frequency data to the PLLs and DDSs serially according to the display frequency.

5. TX-RX unit control signal circuit

The microcomputer sends the mode signal, If filter select signal, power signal, and BPF select signal to the TX-RX unit. It receives meter signals and standby switch signals from the TX-RX unit, displays data on the meters, and performs the transmit operation. The output signal from the microcomputer goes to the serial-to-parallel converter (TC9174F, µPD6345). (Fig. 15)

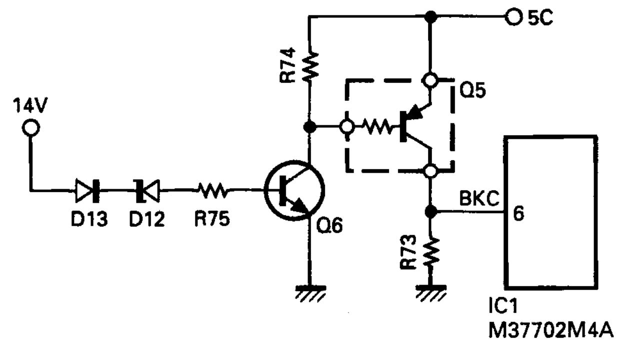


Fig. 14 Backup circuit

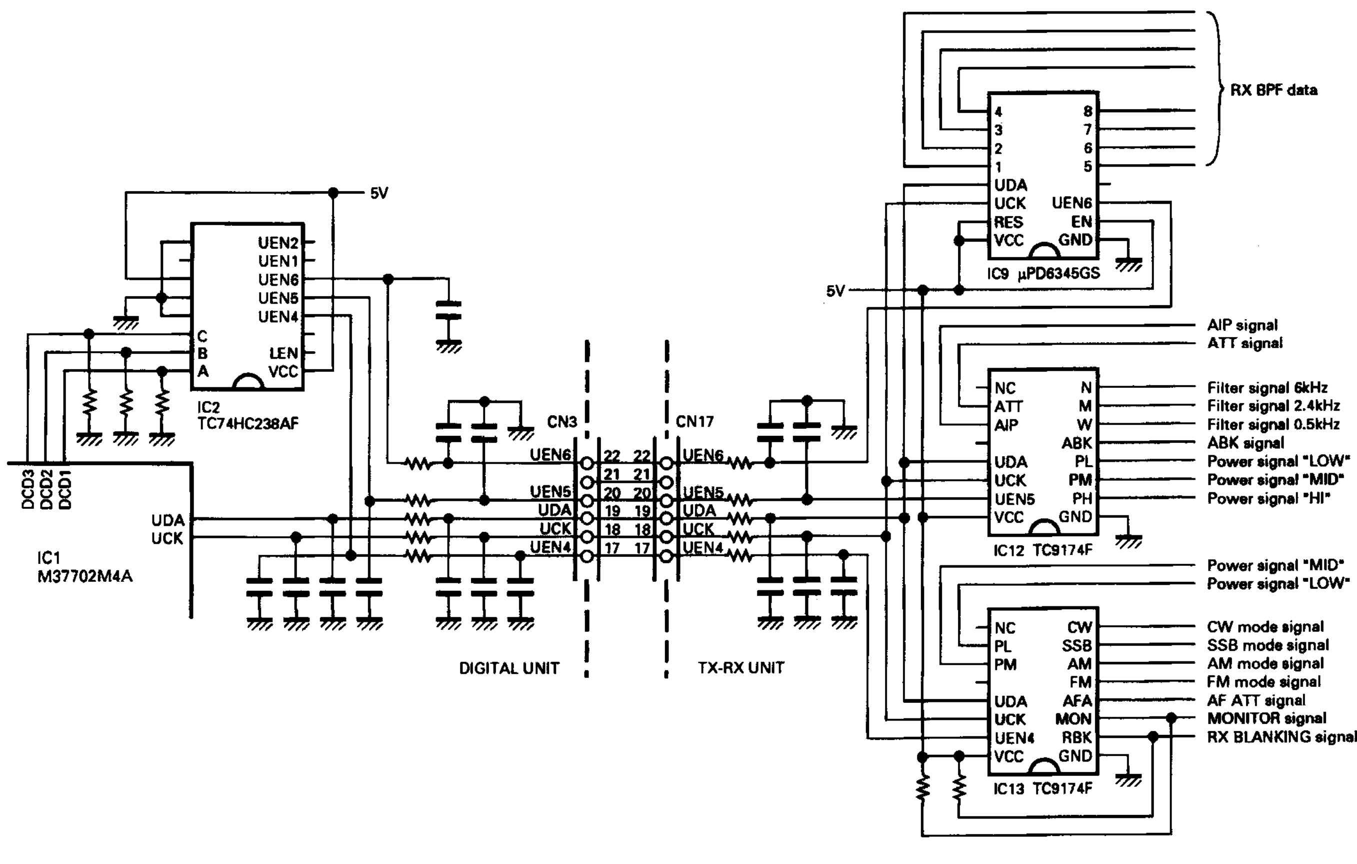


Fig. 15 TX-RX unit control signal circuit

CIRCUIT DESCRIPTION

6. Switch A/D input

The voltage divided by nine switches S16, S2 to S9, S10 to S15, and S17 to S19 is applied to the A/D input pin of the microcomputer when a button is pressed. (Fig. 16) When two or more buttons in the same group are pressed at the same time, only the button with the highest priority is detected (listed below).

KAD1		KAD2		Priority
S16	SPLIT	S11	F. LOCK	1
S3	AIP/AT	S12	DOWN	2
S4	NB	S13	UP	3
S5	RIT	S14	MHz	4
S6	M. IN	S15	A/B	5
S7	SCAN	S10	M/V	6
S8	M>V	S17	A=B	7
S9	CLR	S18	SSB/CW	8
S2	AT TUNE	S19	FM/AM	9

Table 5

7. EEPROM

Adjustment data is stored in the EEPROM, which consists of 256 16-bit registers. Data can be written to and read from the EEPROM. Each time the power is switched on, data is read from the EEPROM. If corrupt data is detected, the default adjustment data is used. Adjustment data can be written into the EEPROM in service adjustment mode. (Fig. 17)

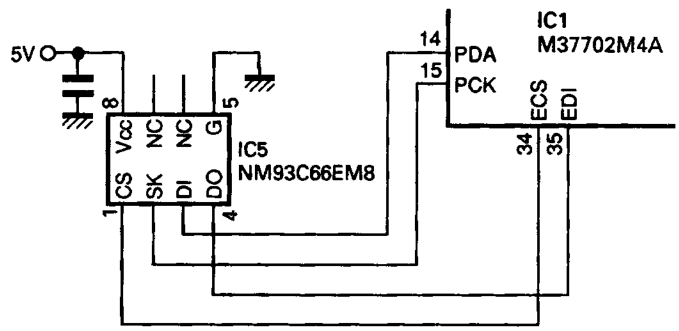


Fig. 17 EEPROM circuit

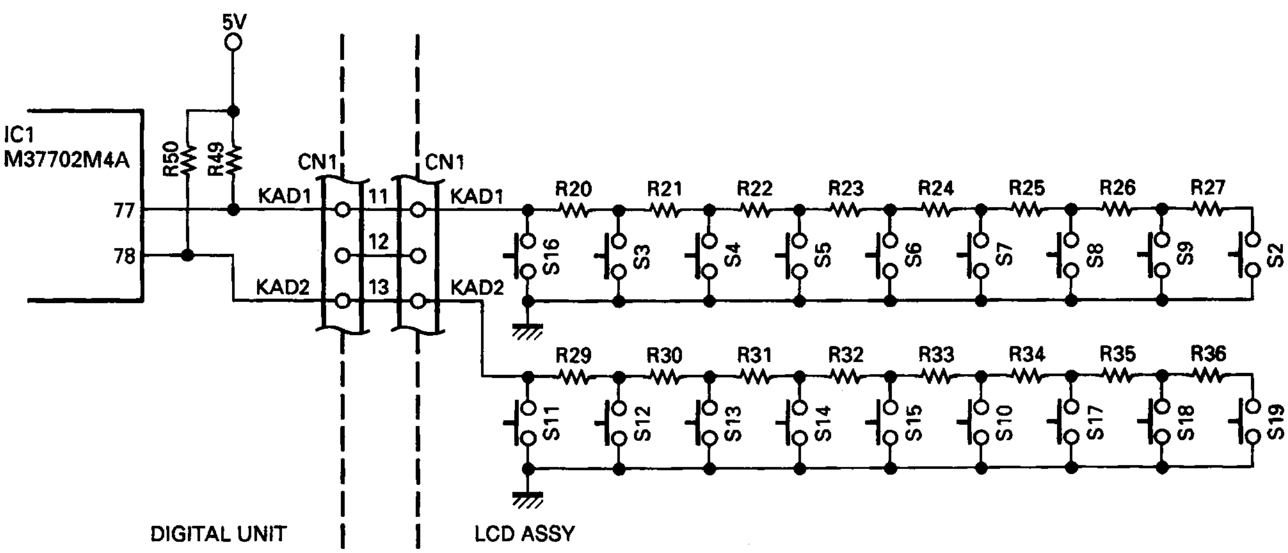


Fig. 16 Switch A/D input circuit

CIRCUIT DESCRIPTION

8. Encoder circuit

The encoder is a mechanical one. The waveforms of the encoder pulses are rectified by IC3 and IC4 (TC4S584F) in the LCD assembly, and the number of pulses is counted by the hardware counter in the microcomputer. The rotational speed of the encoder is detected. When the encoder is turned slowly, the frequency step is made fine; when it is turned quickly, the frequency step is made coarse to ensure smooth tuning and frequency change. The minimum frequency step is 5 Hz (50 Hz in FM mode); the maximum, 200 Hz (2kHz in FM mode). The frequency step is changed continuously according to the speed of rotation. (Fig. 18)

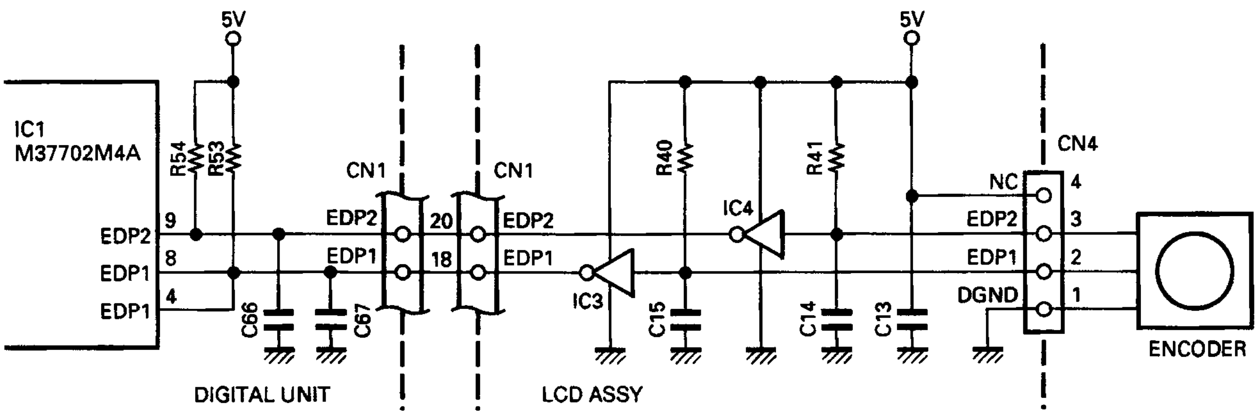


Fig. 18 Encoder circuit

9. Busy signal

The level of the port is monitored in receive mode, and busy indication and busy stop are performed during scanning.

10. Dimmer control

The dimmer is controlled in five steps (including OFF). The lamp is turned on or off by pin 7 of IC2 of the switch unit. The brightness of the dimmer lamp is determined by pins 5 and 6 of IC2. (Fig. 19)

11. Beep

The beep signal is generated using the timer in the microcomputer. The menu enable data (beep on/off, mode beep, warning Morse) is recognized, and the necessary code is output. A dot lasts about 40ms; a dash, about 120ms. The oscillation frequency is about 1.4kHz.

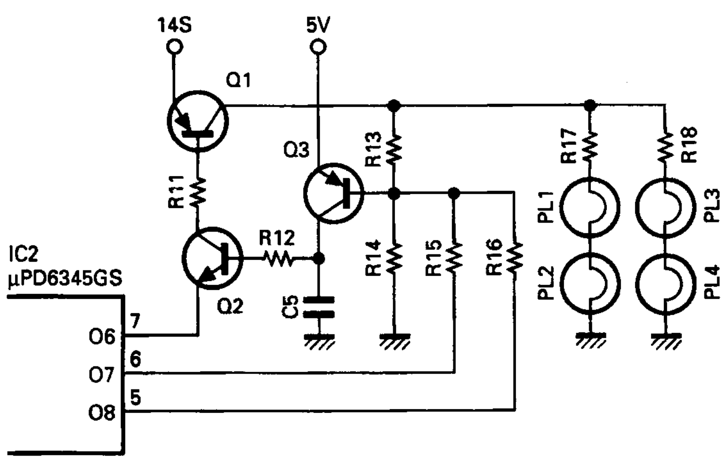


Fig. 19 Dimmer control circuit

CIRCUIT DESCRIPTION

12. Subtone

The subtone frequency is converted from digital to analog by a ladder resistor, and a pseudo-sine wave, including the 1750-Hz tone, is output. (Fig. 20)

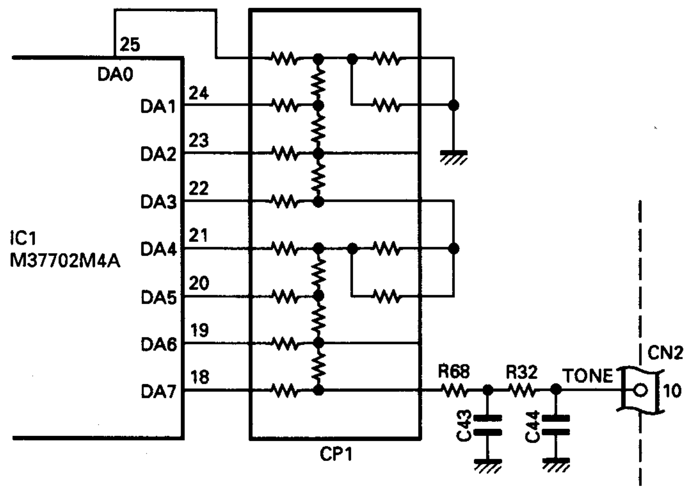


Fig. 20 Subtone circuit

13. AT control signal

The AT-300 (option) control signal is bidirectional, and tuning is done by handshaking with the AT-300. The AT-50 (option) is controlled and tuned by transferring serial data. (Fig. 21)

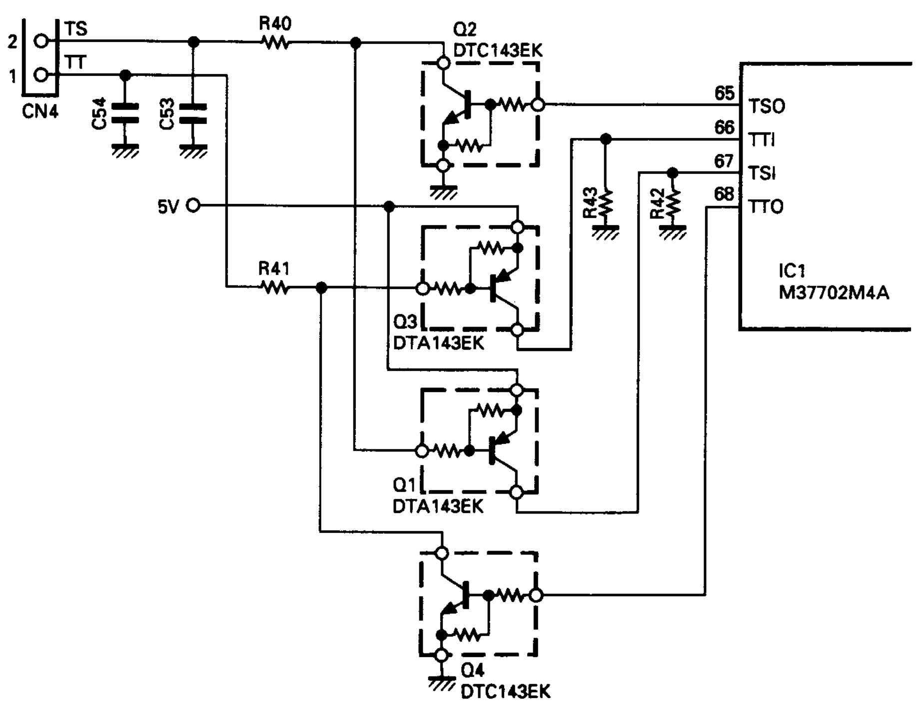


Fig. 21 AT control circuit

CIRCUIT DESCRIPTION

14. Settings

• Contents of menu

If you hold down the F. LOCK key for more than 1.5 seconds, a menu is displayed. You can change the menu number with the encoder, change between menus A and B with the A/B key, and change settings with the UP/DOWN key.

Menu No.	Contents of menu A	State (display)	Initial state
00	Power change	Depending on marketplace	Depending on marketplace
01	Dimmer quantity changeover	OFF/d1/d2/d3/d4	d2
02	AGC SLOW/FAST changeover (SSB, CW, AM)	S/F	Depending on data
03	IF filter switching (SSB, CW, AM)	0.5/2.4/6kHz	Depending on data
04	SSB/CW switch change	SSB/ULC	SSB
05	CW delay time switching	See instruction manual.	600
06	CW pitch change (50-Hz step)	400~1000	800
07	CW reverse on/off	ON/OFF	OFF
08	Encoder lock on/off	ON/OFF	OFF
09	Program scan busy stop on/off	ON/OFF	ON
10	Program scan time-operate/carrier-operate changeover	0/1	0
11	Memory scan busy stop on/off	ON/OFF	ON
12	Memory scan time-operate/carrier-operate changeover	0/1	0
13	All memory scan on/off	ON/OFF	OFF
14	Four times power meter indication at lower power	ON/OFF	OFF
15	Repeater subtone on/off	ON/OFF	ON
16	MIC U/D step frequency change in SSB/CW mode	See instruction manual.	10kHz
17	MIC U/D step frequency change in FM/AM mode	See instruction manual.	10kHz

Menu No.	Contents of menu B	State (display)	Initial state
50	Beep tone on/off	ON/OFF	ON
51	Mode Morse on/off	ON/OFF	ON
52	Warning Morse on/off	ON/OFF	ON
53	Repeater subtone frequency setting	67.0~1750.0	Contents in memory
54	Repeater subtone mode setting	b/c	c
55	Meter peak hold on/off	ON/OFF	ON
56	Memory channel automatic increment on/off	ON/OFF	OFF
57	Standard memory channel frequency temporary change	ON/OFF	OFF
58	Program scan hold function on/off	ON/OFF	OFF
59	Memory protect 1 (write/erase inhibit) on/off	ON/OFF	OFF
60	Memory protect 2 (overwrite/erase inhibit) on/off	ON/OFF	OFF
61	AM broadcast band 9-kHz step function on/off	9kHz/OFF	OFF
62	1-MHz/500-kHz changeover when 1-MHz step is on	1000/500kHz	1000
63	RIT frequency variable range 1.1-kHz/2.2-kHz changeover	1.1/2.2kHz	1.1kHz
64	Automatic power-off on/off	ON/OFF	OFF
65	Transmit inhibit function	ON/OFF	OFF
66	Microphone sensitivity change	H/L	L
67	PF1 key setting	00~99	83 (menu A)
68	PF2 key setting	00~99	00 (power change)
69	PF3 key setting	00~99	36 (TF-SET)
70	PF4 key setting	00~99	82 (monitor)
71	LSB transmit/receive carrier point setting	−100~200	0
72	USB transmit/receive carrier point setting	−100~200	0

CIRCUIT DESCRIPTION

- **PF key functions**

Three kinds of function (panel function, menu A/B function, and non-panel function) are assigned to the four PF keys on the microphone. To assign a function to a key, specify the number in the following table using the UP/DOWN key in the order of 67 to 70 (PF1 to PF4) in menu B mode. The PF keys are named PF1, PF2, PF3, and PF4 from the left, as viewed from the front of the microphone.

No.	Menu A function	No.	Panel key function	No.	Menu B function	No.	Special function
00	Menu 00	20	AT TUNE	50	Menu 50	80	AF MUTE
01	Menu 01	21	AIP	51	Menu 51	81	AF ATT
02	Menu 02	22	ATT	52	Menu 52	82	MONITOR
03	Menu 03	23	NB	53	Menu 53	83	Menu A
04	Menu 04	24	F. LOCK	54	Menu 54	84	Menu B
05	Menu 05	25	UP	55	Menu 55	85	1Hz display
06	Menu 06	26	DOWN	56	Menu 56	99	OFF
07	Menu 07	27	MHz	57	Menu 57		
08	Menu 08	28	RIT	58	Menu 58		
09	Menu 09	29	SCAN	59	Menu 59		
10	Menu 10	30	CLR	60	Menu 60		
11	Menu 11	31	M. IN	61	Menu 61		
12	Menu 12	32	M>V	62	Menu 62		
13	Menu 13	33	M/V	63	Menu 63		
14	Menu 14	34	A/B	64	Menu 64		
15	Menu 15	35	SPLIT	65	Menu 65		
16	Menu 16	36	TF-SET	66	Menu 66		
17	Menu 17	37	A=B				
		38	SSB/CW				
		39	FM/AM				

15.Band data

Frequency	RX BPF DATA								TX LPF DATA						VCO DATA		
(MHz)	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0	LPF6	LPF5	LPF4	LPF3	LPF2	LPF1	VB3	VB2	VB1
0.030000~ 0.499999	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
0.500000~ 0.999999	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
1.000000~ 1.599999	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
1.600000~ 1.999999	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
2.000000~ 2.499999	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
2.500000~ 2.999999	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1
3.000000~ 3.499999	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1
3.500000~ 3.999999	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1
4.000000~ 4.499999	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1
4.500000~ 4.999999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
5.000000~ 5.499999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
5.500000~ 5.999999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1

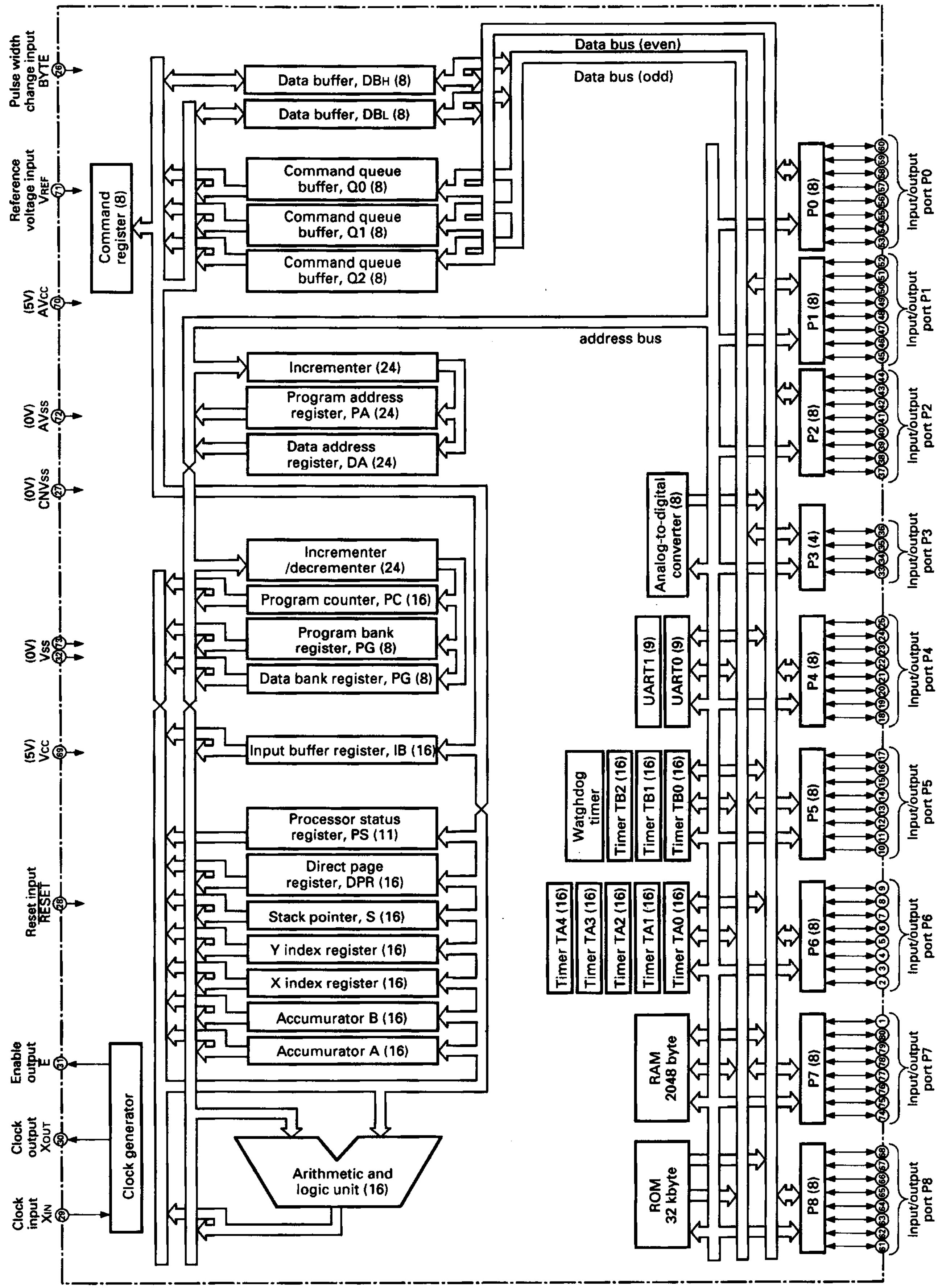
CIRCUIT DESCRIPTION

Frequency (MHz)	RX BPF DATA								TX LPF DATA						VCO DATA		
	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0	LPF6	LPF5	LPF4	LPF3	LPF2	LPF1	VB3	VB2	VB1
6.000000~ 6.499999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
6.500000~ 6.999999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
7.000000~ 7.499999	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
7.500000~ 7.999999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
8.000000~ 8.499999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
8.500000~ 8.999999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
9.000000~ 9.499999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
9.500000~ 9.999999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
10.000000~10.499999	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
10.500000~10.999999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
11.000000~11.499999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
11.500000~11.999999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
12.000000~12.499999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
12.500000~12.999999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
13.000000~13.499999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
13.500000~13.999999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
14.000000~14.499999	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0
14.500000~14.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
15.000000~15.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
15.500000~15.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
16.000000~16.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
16.500000~16.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
17.000000~17.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
17.500000~17.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
18.000000~18.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
18.500000~18.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
19.000000~19.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
19.500000~19.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
20.000000~20.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
20.500000~20.999999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
21.000000~21.499999	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
21.500000~21.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
22.000000~22.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
22.500000~22.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
23.000000~23.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
23.500000~23.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
24.000000~24.400000	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
24.500000~24.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
25.000000~25.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
25.500000~25.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
26.000000~26.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
26.500000~26.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
27.000000~27.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
27.500000~27.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
28.000000~28.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
28.500000~28.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
29.000000~29.499999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
29.500000~29.999999	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

SEMICONDUCTOR DATA

CPU : M37702M4A-FP (Digital Unit IC1)

- **Block diagram**



SEMICONDUCTOR DATA

- **Terminal function**

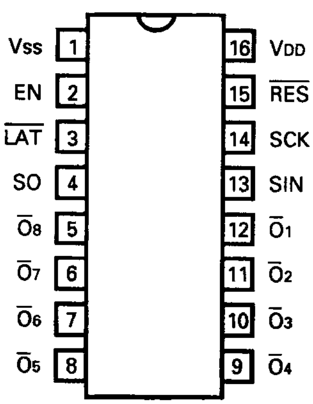
Pin	Pin name	Signal name	I/O	Function	Remarks
1	AN0/	MDN	I	Microphone down switch	/P70
2	P67/	CSS	I	PTT switch	/TB2IN
3	P66/	LDA	O	LCD data	Destination D input strobe/TB1IN
4	TB0IN/	EDP1	I	Encoder pulse	/P65
5	INT2/	LCK	O	LCD clock	/P64
6	INT1/	BKC	I	Backup Vcc detection	/P63
7	INT0/	PSW	I	Power switch	/P62
8	TA4IN	EDP1	I	Encoder pulse	/P61
9	TA4OUT	EDP2	I	Encoder pulse	/P60
10	P57/	DRL	O	Power relay control	/TA3IN
11	P56/	THP	I	Final temperature detection	/TA3OUT
12	P55/	NFT	O	Not FM TX	/TA2IN
13	P54/	PEN2	O	PLL enable	/TA2OUT
14	P53/	PDA	O	PLL/EEPROM/DDS data	/TA1IN
15	P52/	PCK	O	PLL/EEPROM/DDS clock	/TA1OUT
16	P51/	NB	O	NB on/off	/TA0IN
17	P50/	BEEP	O	Beeper pulse	/TA0OUT
18~22	P47~P43	DA7~DA3	O	D/A	
23	P42/	DA2	O	Digital-to-analog converter	/ø
24	P41/	DA1	O	Digital-to-analog converter	/RDY
25	P40/	DA0	O	Digital-to-analog converter	/HOLD
26	BYTE		I	(External bus width specification)	* = don't care
27	CNVss		I	CPU operation mode specification	
28	RESET	RES	I	CPU reset	
29	XIN		I	System clock	
30	XOUT		O	System clock	
31	E		O		
32	Vss				
33	P33/	DEN2	O	DDS2 enable	/HLDA
34	P32/	ECS	O	EEPROM chip select	/ALE
35	P31/	EDI	I/O	EEPROM data output/Busy input	/BHE
36	P30/	UCK	O	Shift register clock	/R/W
37	P27/	UDA	O	Shift register data	/A23/D7
38	P26/	KYS	I	Key jack input	/A22/D6
39	P25	KYB	I	Key input	/A21/D5
40	P24/	TXS	O	TX/RX control	/A20/D4
41	P23/	RXS	O	RX enable	/A19/D3
42	P22/	CKS	O	CKY control signal	/A18/D2
43	P21/	AGC	O	AGC slow/fast changeover	/A17/D1
44	P20/	HEN	O	Latch enable	/A16/D0
45~52	P17/~P10	D7~D0	I/O	Pseudo-bus	/A15/D15~/A8/D8
53	P07/	BSY	I	Signal busy	/A7
54	P06/	MGS	O	Microphone sensitivity selection	/A6
55	P05/	ULK	I	Unlock signal	/A5
56	P04/	PEN1	O	PLL enable	/A4
57	P03/	DEN1	O	DDS1 enable	/A3
58~60	P02/~P00/	DCD1~DCD3	O	Decoder output	/A2~/A0
61	P87/	TXD	O	ASCI (debug)	/TXD1
62	P86/	RXD	I	ASCI (debug)	/RXD1
63	P85/	RTS	O	ASCI (debug)	/CLK1
64	P84/	CTS	I	ASCI (degub)	/CTS1/RTS1
65	TXD0/	TSO	O	AT TS signal	Connection with TSI/P83
66	RXD0	TTI	I	AT TT signal	Connection with TTO/P82

SEMICONDUCTOR DATA

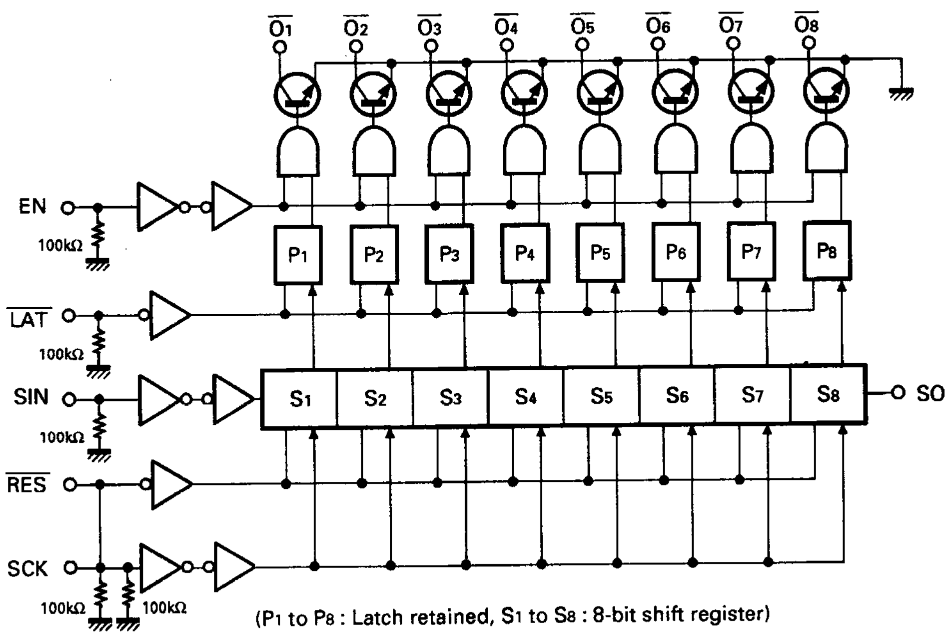
Pin	Pin name	Signal name	I/O	Function	Remarks
67	P81/	TSI	I	AT TS signal	Connection with TSO/CLK0
68	CTS0/	TTO	O	AT TT signal	Connection with TTI/P80/RTS0
69	Vcc		I	Power supply	
70	AVcc		I	Analog-to-digital converter power supply	
71	VREF		I	Analog-to-digital converter reference power supply	
72	AVss		I	Analog-to-digital converter ground	
73	Vss		I	Ground	
74	AN7/	SM	I	Signal strength meter	/P77/ADTRG
75	AN6/	PWM	I	Power meter	/P76
76	AN5/	RVR	I	RIT VR	/P75
77, 78	AN4/, AN3/	KAD1, KAD2	I	Panel key input	/P74, /P73
79	AN2/	ISV	I	IF SHIFT VR	/P72
80	AN1/	MUP	I	Microphone up switch	

Extended I/O : μPD6345GS (TX-RX Unit IC9)

- **Terminal connection diagram**



- **Block diagram**



(P1 to P8 : Latch retained, S1 to S8 : 8-bit shift register)

- **Terminal function**

Pin No.	Code	Pin name	I/O	Function
1	GND	Ground pin	–	Connected to system ground.
2	EN	Enable pin	I	High : Data is output; Low (or open) : All output buffers are turned off.
3	$\overline{LAT}$	Latch pin	I	Low (or open) : Data is retained; High : Data is latched.
4	SO	Serial data output pin	O	Serial data is output on rising edge of SCK. If no μPD6345s are connected in series, this pin can be connected to SIN at the next stage.
5~12	$\overline{O_8}$~$\overline{O_1}$	Data output pin	O	Open collector NPN transistor high-voltage-resistant output. Correspond to outputs $\overline{Q_1}$ to $\overline{O_8}$.
13	SIN	Serial data input pin	I	Data input pin : Input to shift register on rising edge of SCK.
14	SCK	Serial clock input pin	I	SIN data is read into the shift register on rising edge of SIN; data is output from SO on rising edge of SCK.
15	$\overline{RES}$	Reset input pin	I	All shift register data is cleared. High : Normal operation; Low (or open) : Reset.
16	VDD	Power supply pin	–	4 to 6V.

SEMICONDUCTOR DATA

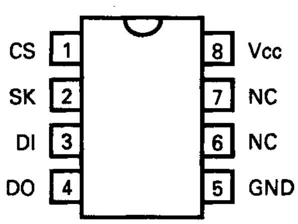
- **Truth table**

SCK	EN	$\overline{RES}$	$\overline{LAT}$	SIN	OUT		SO *1	Remarks
					$\overline{O_1}$	$\overline{O_8}$		
↑	H	H	H	L	High impedance	$\overline{O_{8-1}}$	S_7	SCK : Clock input E : Enable input
↑	H	H	H	H	L	$\overline{O_{8-1}}$	S_7	$\overline{RES}$: Reset input $\overline{LAT}$: Latch input
↑	H	H	L *2	*	No change	No change	S_7	SIN : Serial input
↑	L	H	*	*	High impedance	High impedance	S_7	OUT : Parallel output
↓	*	*	*	*	No change	No change	S_8	SO : Serial output * : H or L
*	*	L	H	*	High impedance	High impedance	L	H : High level L : Low level
*	H	⊔	L	*	No change	No change	L	

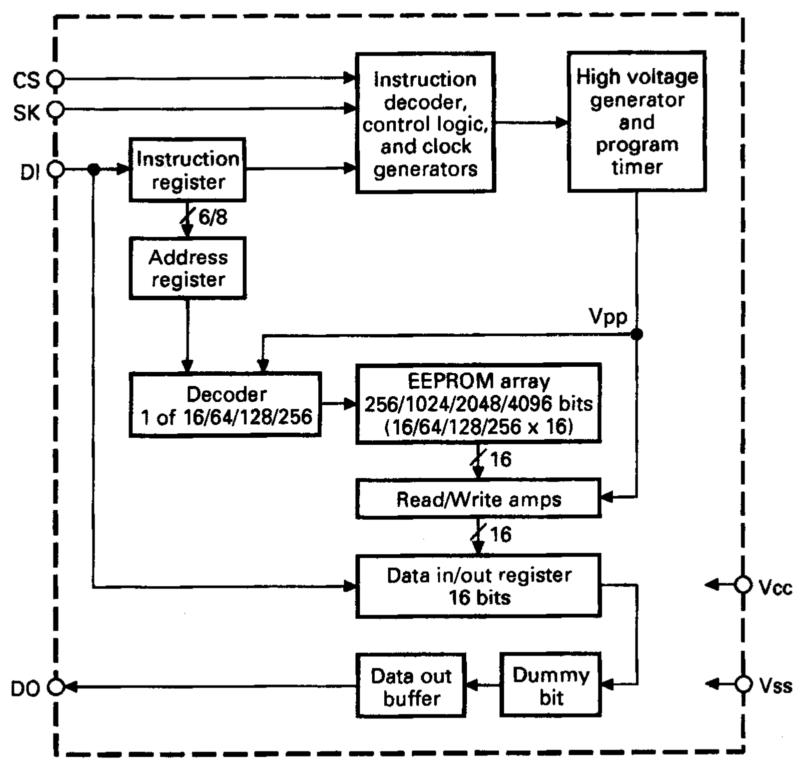
*1 : Data S_7 is shifted to data S_8, and data is output to SO output on rising edge of clock.
*2 : The shift register is executed.

EEPROM : NM93C66EM8 (Digital Unit IC5)

- **Terminal connection diagram**



- **Block diagram**



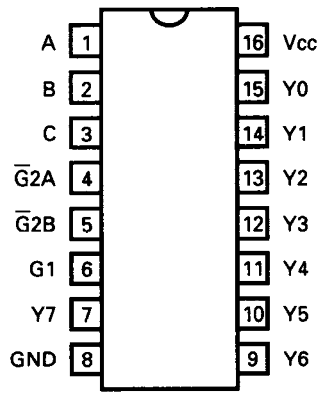
- **Terminal names**

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

SEMICONDUCTOR DATA

3 to 8 Line Decoder : TC74HC238AF (Digital Unit IC2)

- **Terminal connection diagram**



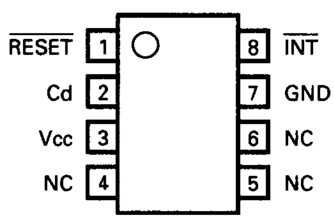
- **Truth table**

Inputs						Outputs								Selected output
Enable			Select											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
L	X	X	X	X	X	L	L	L	L	L	L	L	L	None
X	H	X	X	X	X	L	L	L	L	L	L	L	L	None
X	X	H	X	X	X	L	L	L	L	L	L	L	L	None
H	L	L	L	L	L	H	L	L	L	L	L	L	L	Y0
H	L	L	L	L	H	L	H	L	L	L	L	L	L	Y1
H	L	L	L	H	L	L	L	H	L	L	L	L	L	Y2
H	L	L	L	H	H	L	L	L	H	L	L	L	L	Y3
H	L	L	H	L	L	L	L	L	L	H	L	L	L	Y4
H	L	L	H	L	H	L	L	L	L	L	H	L	L	Y5
H	L	L	H	H	L	L	L	L	L	L	L	H	L	Y6
H	L	L	H	H	H	L	L	L	L	L	L	L	H	Y7

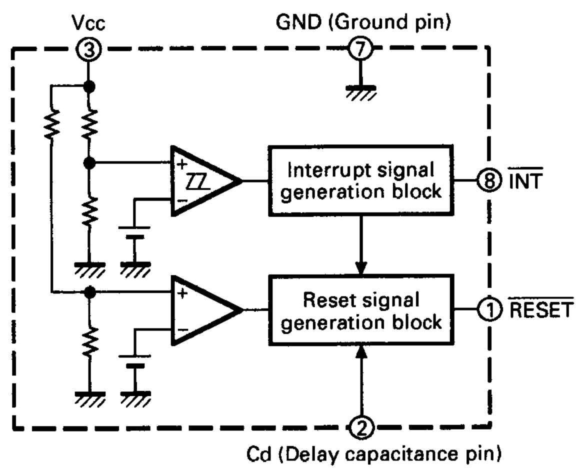
X : Don't care

System Reset : M62003FP (Digital Unit IC4)

- **Terminal connection diagram**



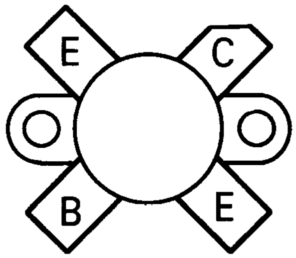
- **Block diagram**



SEMICONDUCTOR DATA

Final Transistor : 2SC2879 (Final Unit Q5, 6)

- External View

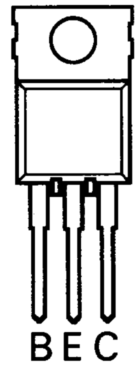


- **Maximum rating** (Ta = 25°C)

Item	Symbol	Rating	Unit
Collector-Base voltage	V_{CBO}	45	V
Collector-Emitter voltage	V_{CES}	45	V
Collector-Emitter voltage	V_{CEO}	18	V
Emitter-Base voltage	V_{EBO}	4	V
Collector current	I_C	25	A
Collector dissipation (Tc=25°C)	P_C	250	W
Operating temperature	Tj	175	°C
Storage temperature	Tstg	−65~+175	°C

Drive Transistor : 2SC3133 (Final Unit Q2, 3)

- External View



- **Maximum rating** (Ta = 25 ± 3°C)

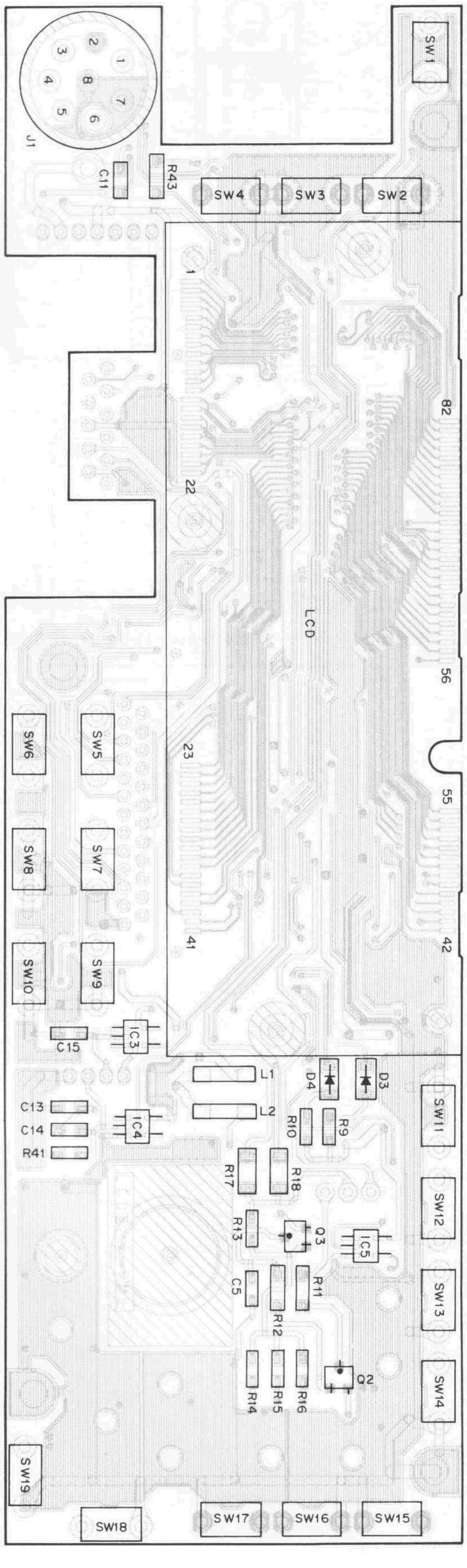
Symbol	Condition	Rating	Unit
V_{CBO}		60	V
V_{EBO}		5	V
V_{CEO}	$R_{BE} = \infty$	25	V
I_C		6	A
P_C	Tc = 25°C	20	W
Tj		150	°C
Tstg		−55~+150	°C

SEMICONDUCTOR DATA

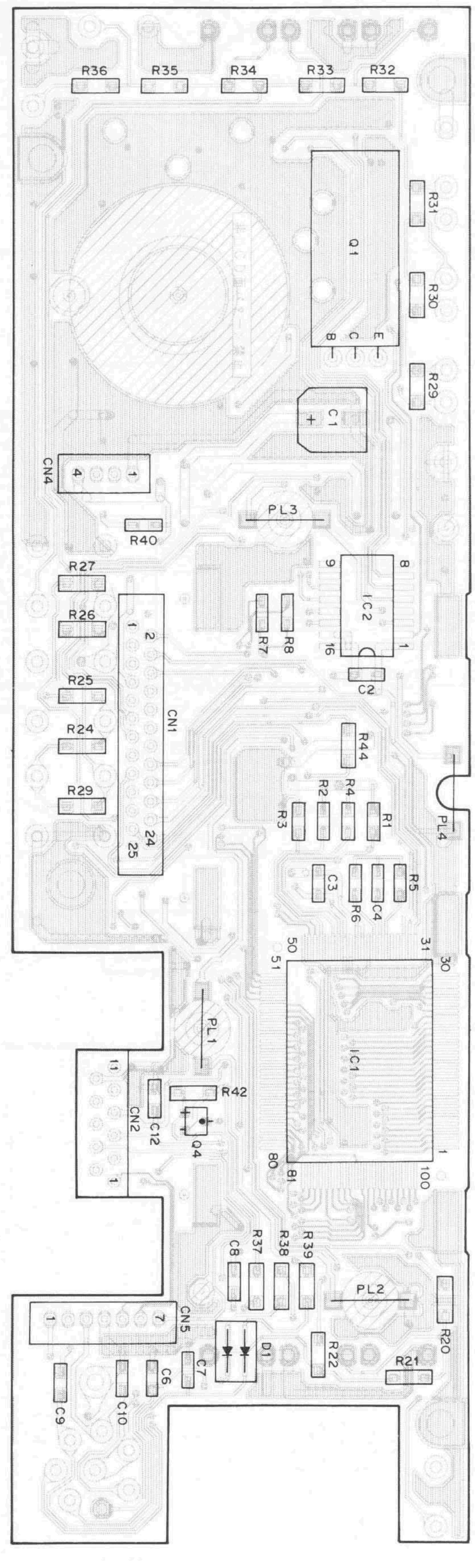
LCD Assy : B38-0377-05

- **PC board views (SW unit)**

Component side view

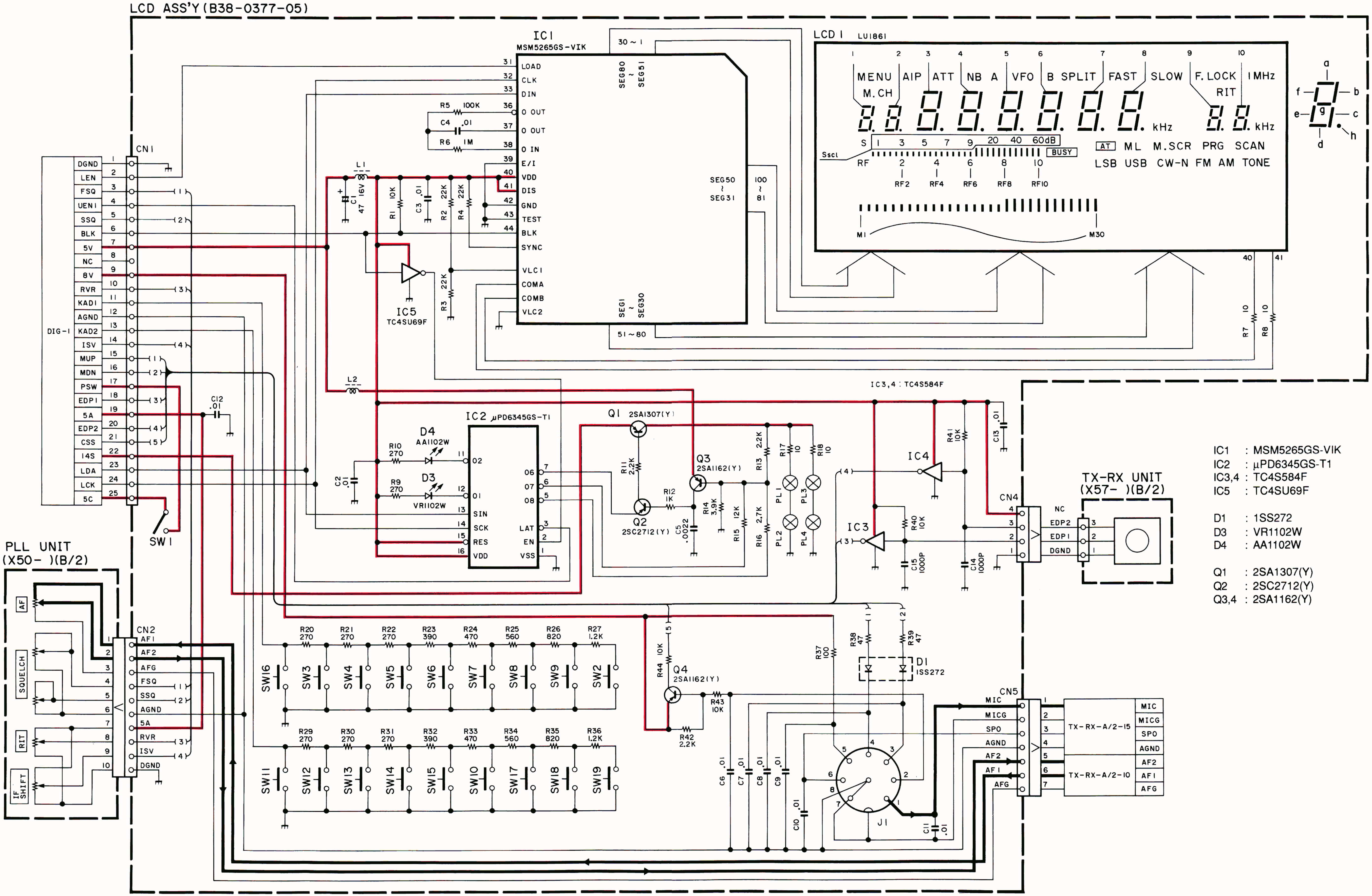


Foil side view



SEMICONDUCTOR DATA

- **Schematic diagram**



Kenwood page numbering..

Page 30 is part of p29 above. This is a placeholder to keep page numbers consecutive.