HF TRANSCEIVER/MULTI BANDER

TS-140S/680S

SERVICE MANUAL

KENWOOD

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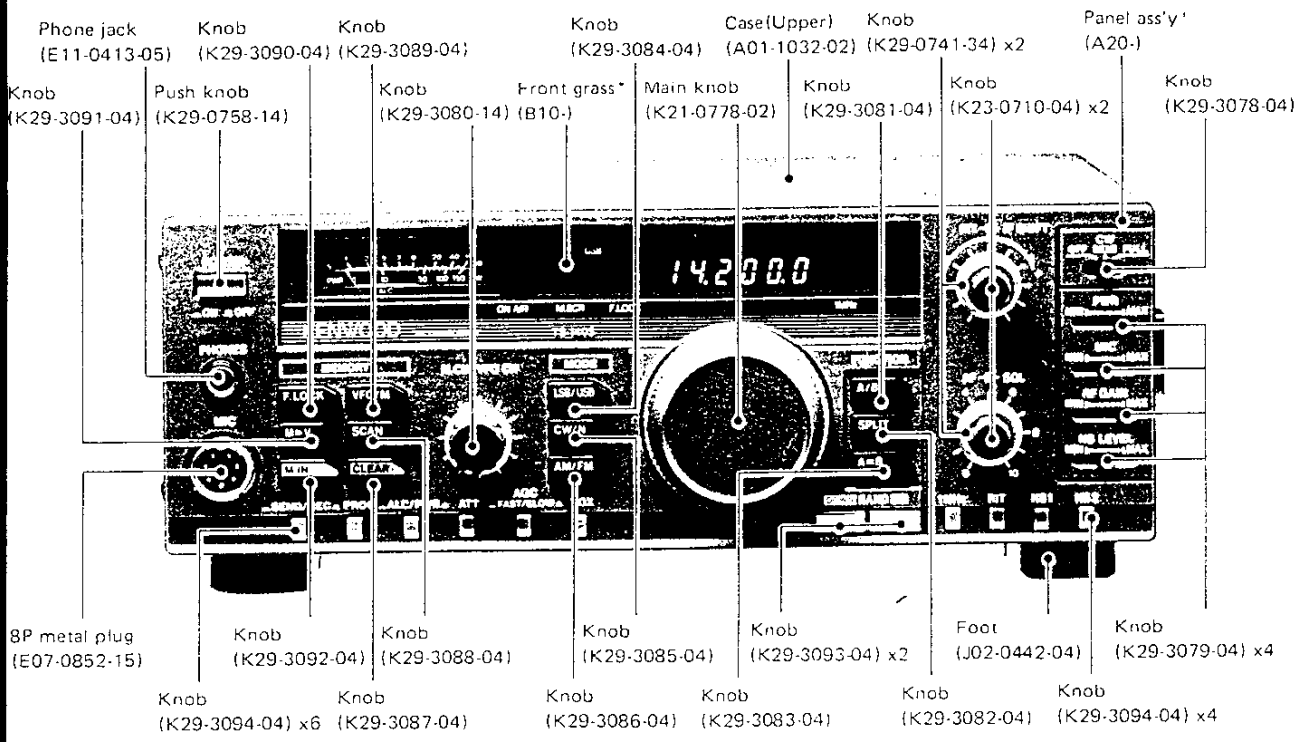


*Refer to parts list on page 42.

CONTENTS

CIRCUIT DESCRIPTION

Note: This text is concerned primarily with the TS-140. those parts that pertain to the TS-680 will be marked with an asterisk (*).

GENERAL

The TS-140 is a transceiver incorporating a general coverage receiver section utilizing double conversion principles with a first intermediate frequency (IF) of 40.005 MHz and a second IF of 455kHz.

The TS-140 covers all amateur bands from 1.9MHz to 30MHz (*1.9 thru 50MHz). It contains a 10Hz step digital PLL circuit using single crystal frequency management and microprocessor control to provide high accuracy and stability.

The major functions are as follows:

- Receiving section: General coverage from 500kHz to 30 MHz (*500kHz to 30MHz, and 50 to 54MHz)
- Covers all amateur bands from 1.9 to 30MHz (*1.9 to 54 MHz)
- Full CW break-in
- 28MHz (*50MHz) band Preamplifier control
- Manual switching of AGC time constsnt
- Built-in variable threshold noise blanker
- Built-in woodpecker noise blanker (NB2)
- Frequency control function with a second sub-control
- Frequency configured using a single reference oscillator
- Range specified memory

FREQUENCY CONFIGURATION

The TS-140 operates using a double conversion syst for both transmit and receive (it operates using single c version in the FM transmit mode).

Figure 1 shows the frequency configuration of t transmit and receive systems. The receiver section will covered first.

Assume that the input frequency from the antenna fIN, the RX MIX1 local input is fVCO, and the RX MI local input is fHET. When the incoming signal is zero be the following relationships will hold true.

$$f_{IN} = f_{VCO} - f_{HET} - f_{CAR} \quad \cdots\cdots (1)$$

for VCO4, $\frac{f_{VCO4}}{J} = \frac{f_{STD}}{8K}$ $\therefore f_{VCO4} = \frac{J}{8K} f_{STD}$ $\cdots\cdots (2)$

for VCO3, $\frac{f_{VCO3}}{L} = \frac{f_{STD}}{8 \times 900}$ $\therefore f_{VCO3} = \frac{L}{7200} f_{STD}$ $\cdots\cdots (3)$

for VCO2, $\frac{f_{VCO2}}{M} = \frac{f_{STD}}{8 \times 4500}$ $\therefore f_{VCO2} = \frac{M}{36000} f_{STD}$ $\cdots\cdots (4)$

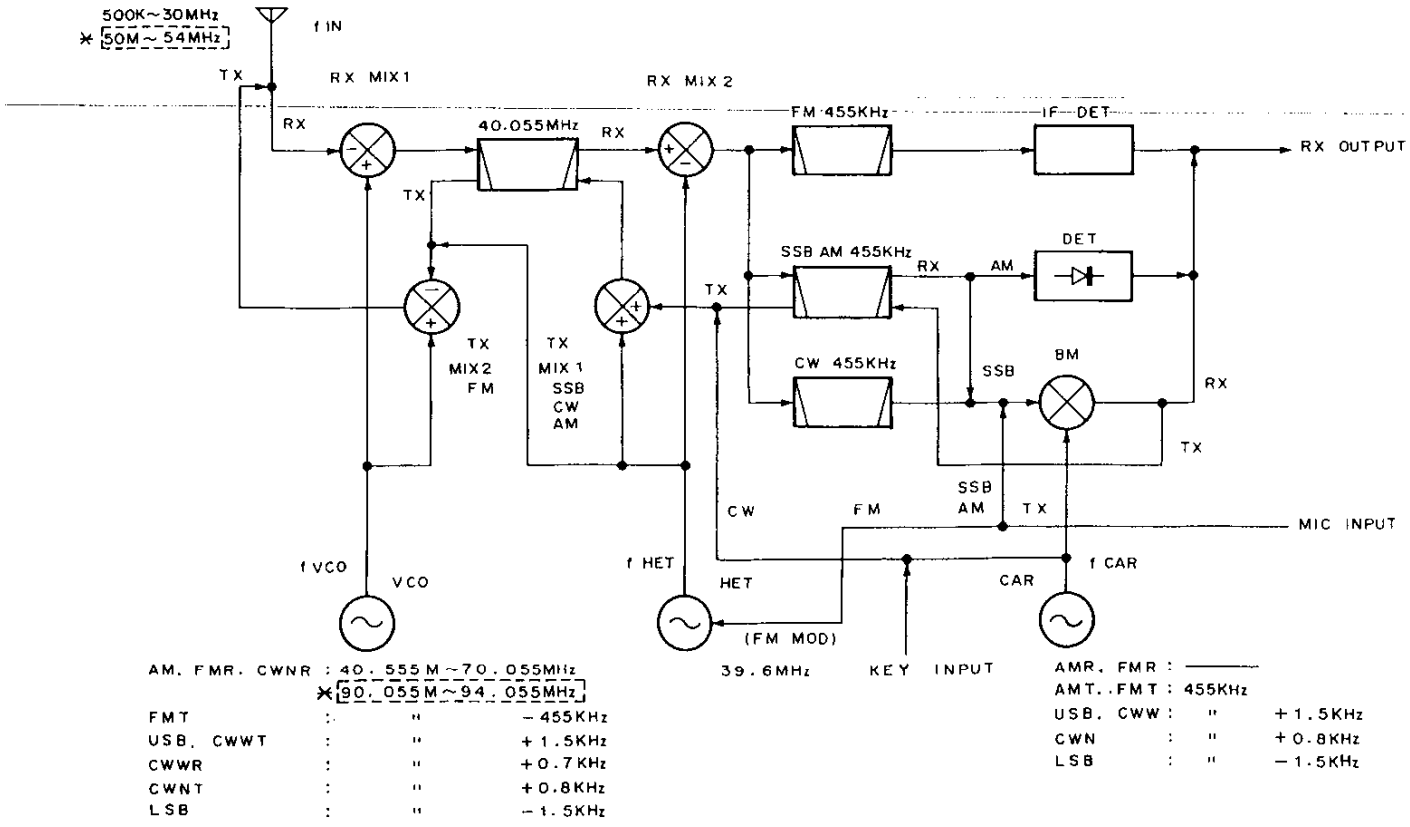


Fig. 1 Signal system frequency configuration

CIRCUIT DESCRIPTION

for VCO1, in the range of 500kHz to 30MHz

$$\frac{f_{VCO1}-\left(\frac{f_{VCO2}}{100}+\frac{f_{VCO3}}{200}+\frac{f_{STD}}{8}+f_{STD}-\frac{f_{STD}}{8}\right)}{N}=\frac{f_{STD}}{8\times 90}$$

$$\therefore f_{VCO1}=\left(\frac{N}{720}+\frac{M}{3600000}+\frac{L}{1440000}+1\right)f_{STD}\cdots\cdots⑤$$

Each local oscillator frequency may be summarized as follows:

$$f_{VCO}=f_{VCO1}\cdots\cdots⑥$$

$$f_{HET}=f_{VCO4}\cdots\cdots⑦$$

$$f_{CAR}=\frac{f_{VCO3}}{200}=\frac{L}{1440000}f_{STD}\cdots\cdots⑧$$

Therefore, f_{IN} in equation (1) is expressed as follows:
VCO1-A: 500kHz to 10.5MHz:

$$f_{IN}=\left(\frac{N}{720}+\frac{M}{3600000}-\frac{J}{8K}+1\right)f_{STD}\cdots\cdots⑨$$

Similarly, VCO1-B and VCO1-C are represented as follows:
VCO1-B: 10.5MHz to 21.5MHz:

$$f_{IN}=\left(\frac{N}{720}+\frac{M}{3600000}-\frac{J}{8K}+\frac{9}{8}\right)f_{STD}\cdots\cdots⑩$$

VCO1-C: 21.5MHz to 30MHz:

$$f_{IN}=\left(\frac{M}{3600000}-\frac{N}{720}-\frac{J}{8K}+\frac{17}{8}\right)f_{STD}\cdots\cdots⑪$$

*VCO1-D: 50MHz to 54MHz:

$$f_{IN}=\left(\frac{N}{720}+\frac{M}{3600000}-\frac{J}{8K}+\frac{17}{8}\right)f_{STD}\cdots\cdots⑫$$

As we have shown in equations (9) to (12) above the term fCAR can be eliminated, therefore the receive frequency is determined only by the reference fSTD and division ratios J to N (except L) (*J,K,M and N).

These equations may be further analyzed as follows:

(1) The division ratios are determined according to the desired operating frequency, by the microprocessor, and can be assumed to essentially contain no errors.
(2) Since each relationship is expressed using the fSTD linear equation, the reference frequency accuracy equals the operating frequency accuracy.
(3) The operating frequency remains unchanged even when the value of L changes.

When f_{IN} = 14MHz (USB) equation (10) is as follows:
J = 180, K = 1,584, L = 18,260, M = 55,000, N = 251
Therefore, f_{IN} = 1.25 fSTD.....⑬
When f_{IN} = 29.99999MHz (USB) equation (11) is as follows:
J = 180, K = 1,584, L = 18,260, M = 59,999, N = 149
Therefore, f_{IN} = 1.82 fSTD.....⑭
*When f_{IN} = 53.99999MHz (USB) equation (12) is as follows:
J = 180, K = 1,584, L = 18,260, M = 59,999, N = 330
Therefore, f_{IN} = 2.49 fSTD.....⑮

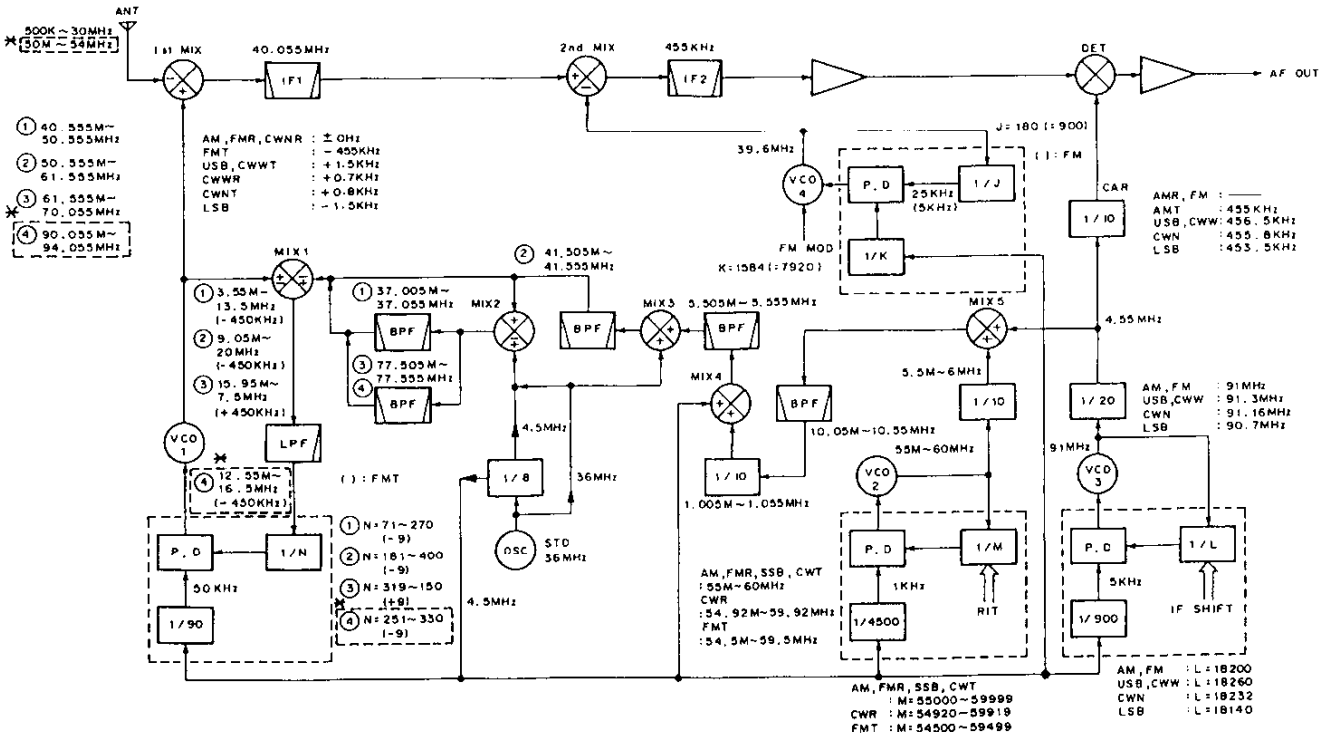


Fig. 2 PLL system frequency configuration

CIRCUIT DESCRIPTION

Since the accuracy of the reference crystal oscillator used in the TS-140 is 10PPM (−10 to +50 deg C), the overall accuracy is obtained by equations (9) to (12) according to characteristics (1) and (2). It is ±450Hz for 14MHz, and ±660Hz maximum for the frequency range of 500kHz to 30MHz. The accuracy of the transceiver is very stable.

*The total accuracy is ±900Hz at maximum for 50 to 54 MHz.

The variable band functions such as the IF shift are controlled by the microprocessor, by cotrolling the value of L, thus taking advantage of the characteristics (3). The carrier point setting and initial IF shift setting are adjusted by fine tuning of fCAR.

The receive frequency in SSB mode has been discussed already. In the other modes and during transmit operations the other modes and during transmit operations frequency is determined by the reference and division rations in the same manner as in the SSB mode in.

For CW receive the fVCO frequency is shifted down 800Hz at fVCO2.

For FM transmit the fVCO frequency is shifted down 455Hz at fVCO1 and fVCO2. The audio signal from the microphone is applied to VCO4, and fHET is directly modulated.

fCAR is stabilized by shift data During transmit and receive in the AM mode, and during receive in the FM mode.

The displayed frequency in each mode is listed in table 1.

Mode	Display frequency
USB, LSB	Carrier point frequency
CW	Transmit carrier frequency
AM, FM	IF filter center frequency

Table 1 Display frequencies in modes

Receive Circuit Configuration

The TS-140 receive system operates using double conversion with a first IF of 40.055MHz and a second IF of 455kHz.

The incoming signal from the ANT terminal passes through the filter unit LPF (Low Pass Filter) and transmit/receive switching relay, and is then applied to the RAT terminal of the signal unit. This signal passes through the 20dB attenuator circuit and an IF trap, and enters the 7 part HPF (High Pass Filter) (BPF for 1.6 to 2.5MHz). It combines with the LPF of the filter unit to give the required band rejection for each band.

*When the signal passes through the HPF, the preamplifier can be turned off or on via relays controlled by Q70 (2SK125-5) and Q71 (2SC1907) for 21.5 to 30 MHz or Q72 (2SK125-5) for 50 to 54MHz. When the preamplifier is turned on the signal is amplified approximately 10dB. For 50 to 54MHz the signal passes through buffer amplifier Q73 (2SC1907) for impedance matching regardless of the preamplifier state.

The signal passes through the IF trap again, and is combined with the VCO (Voltage Controlled Oscillator) in the first mixer, Q18 and Q19 (2SK125-5), to generate the first UF of 40.055MHz. The VCO circuit consits of Q9 thru Q11 (2SC2668Y), and generates 40.555 thru 70.055MHz by dividing it into three bands. The frequency is controlled by the DC signal (VCV) from the control unit.

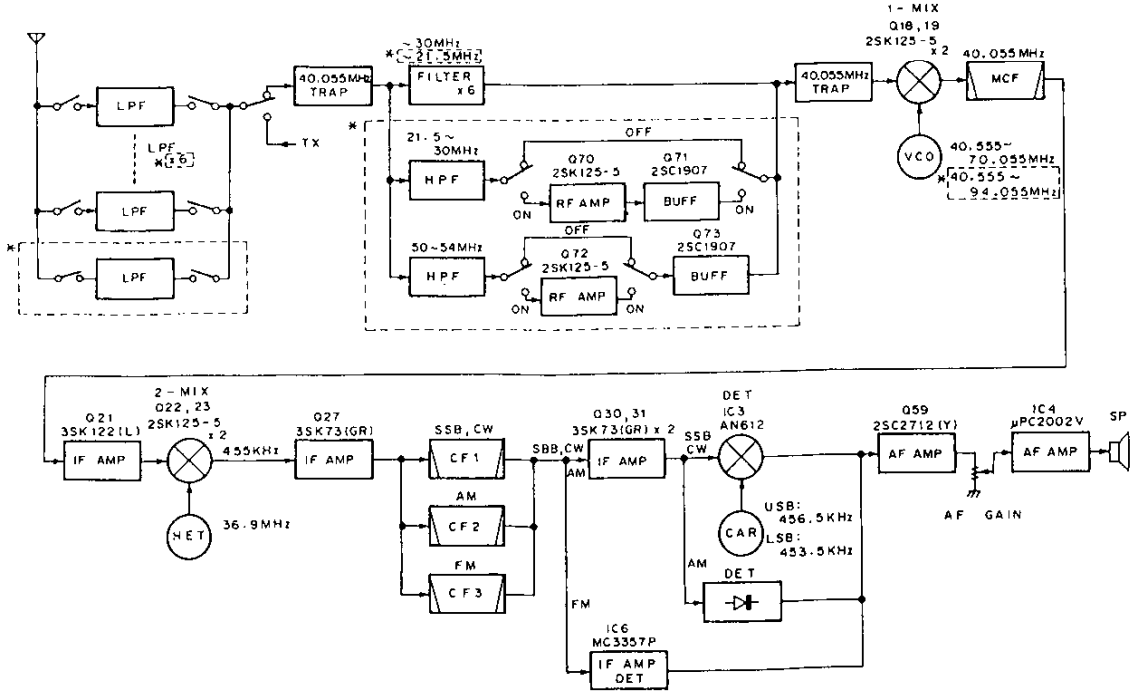


Fig. 3 Receive circuit configuration

CIRCUIT DESCRIPTION

*90.055 to 94.055MHz is generated by the VCO Q12 (2SK192A GR *J). Theerefore the circuit contains four VCO's.

The first IF signal of 40.055MHz passes through the two stage MCF (Monolithic Crystal Filter) that is used in both transmit and receive, and is then amplified by the first IF amplifier Q21 (3SK122L), mixed with the 39.6MHz heterodyne signal by the second mixer, Q22 and Q23 (2SK125-5), to generate the second IF of 455kHz. The heterodyne signal is generated by the control unit, then amplified for use by Q78 (2SK73GR). One portion of the 455kHz signal is applied to the noise blanker amplifier, and the other is amplified by Q27 (2SK73GR), passed through the mode specific ceramic filter (CF1 to CF3) or an optional filter to generate the necessary bandwidth, divided into appropriate mode, and fed into each amplifier circuit.

In modes other that FM, the signal is amplified by IF amplifier Q30 and Q31 (3SK73GR), detected by IC3 (AN612) for SSB and CW, and envelope detected by D75 for the AM mode.

In the FM mode the signal is trasmitted to IC6 (MC3357P) for limiting, amplification, and detection. This circuit is noise squelch cotrolled.

The AF signal in each mode after detection is selected by analog switch IC7 (TC4066BP), amplified by Q56 (2SC 2717Y), applied to the AF volume control, and amplified the final level by IC4 (μPC2002V).

Item	Rating
Nominal center frequency (fo) and declination	40.055MHz ± 0.75kHz or more
Pass bandwidth	fo ± 7.5kHz or more at 3dB
Attenuation bandwidth	fo ± 25kHz or more at 30dB fo ± 150kHz or more at 60dB Spurious is 30dB or more
Guaranteed attenuation	60dB or more at fo ± 150kHz ~ fo ± 1000kHz
Ripple	1.5dB or less
Insertion loss	4dB or less
I/O termination impedance	4.2kΩ

Table 2 MCF (L71-0275-05) (Signal unit XF1)

Item	Rating
Center frequency at 6dB	455kHz ± 0.20kHz
6dB bandwidth (total)	± 1.1 ~ ± 1.3kHz
60dB bandwidth	4.5kHz or less
Guaranteed attenuation (0.1 ~ 1MHz)	60dB or more
Spurious (600 ~ 700kHz)	40dB or more
Ripple at 6dB bandwidth	2dB or less
Insertion loss	2dB or less
I/O termination impedance	2kΩ

Table 3 Ceramic filter (L72-0356-05) (Signal unit CF1)

Item	Rating
Mominal center frequency (fo)	455kHz
6dB bandwidth	± 2kHz or less
40dB bandwidth	± 7.5kHz or less
Insertion loss	6dB or less
Guaranteed attenuation (Within fo ± 100Hz)	35dB or more
I/O termination impedance	2.0kΩ

Table 4 Ceramic filter (L72-0355-05) (Signal unit CF2)

Item	Rating
Nominal center frequency (fo)	455kHz ± 1kHz
6dB bandwidth (From 455kHz)	± 6kHz or more
50dB bandwidth (From 455kHz)	± 12.5kHz or less
Ripple (Within fo ± 4kHz)	3dB or less
Insertion loss	6dB or less
Guaranteed attenuation (Within fo ± 100kHz)	35dB or more
I/O termination impedance	2.0kΩ

Table 5 Ceramic filter (L72-0315-05) (Signal unit CF3)

Noise Blanker Circuit

NB1

NB1 is a noise blanker circuit which is designed for short duration noise interference such as might be encountered in an automobile. The 455kHz IF signal generated from the first IF of 40.055MHz by the second MIX is amplified by the noise amplifiers Q45, Q46, Q47 (2SC2712Y), buffered by Q48, and noise detected by D86. This signal switches Q51 (2SC2712Y), turns on Q28 (2SA1162Y) and Q29 (2SC2712Y), and switches the IF signal line according to variations in the incoming noise.

When NB1 turns on, a DC voltage is applied to the emitter of Q51 from the threshold cotrol, VR4. The effect of the noise blanker is cotrolled by varying this emitter voltage.

CIRCUIT DESCRIPTION

NB2

NB2 is a noise blanker circuit which blanks noises that have a relatively long duration, such as is generated by the so caslled "Russian Woodpecker". The noise signal is first amplified by noise amplifiers Q45 thru Q47, and then detected by D87, just as occurs with NB1. The threshold voltage on the emitter of Q50 (2SC2712Y) is also controled by VR4. Q50's output enters the NB2 module unit X59-3350-00 to synchronize pulse width and period signals with the woodpecker noise.

1/4,4/4 and 2/4,3/4 of IC1 (TC4011BF), are adjusted to a pulse width of 40ms.

Normally, woodpecker type noise has a pulse width of 3 to 4ms and a period of 80 to 100ms, but some woodpecker noise signals might have a period of approximately 50ms, although rare.

Therefore, even woodpecker noise with a large pulse width can be blanked by switching the noise at a 5ms rate. However, if noise with a period of several ms is encountered, such as ignition noise, and is blanked at this same interval, then the signal level will drop or become zero. To prevent this from occurring a one-shot multivibrator, composed of IC1 2/4,3/4, is utilized so that the next pulse does not occur until after a delay of 40ms, from the last output from IC1 1/4,4/4.

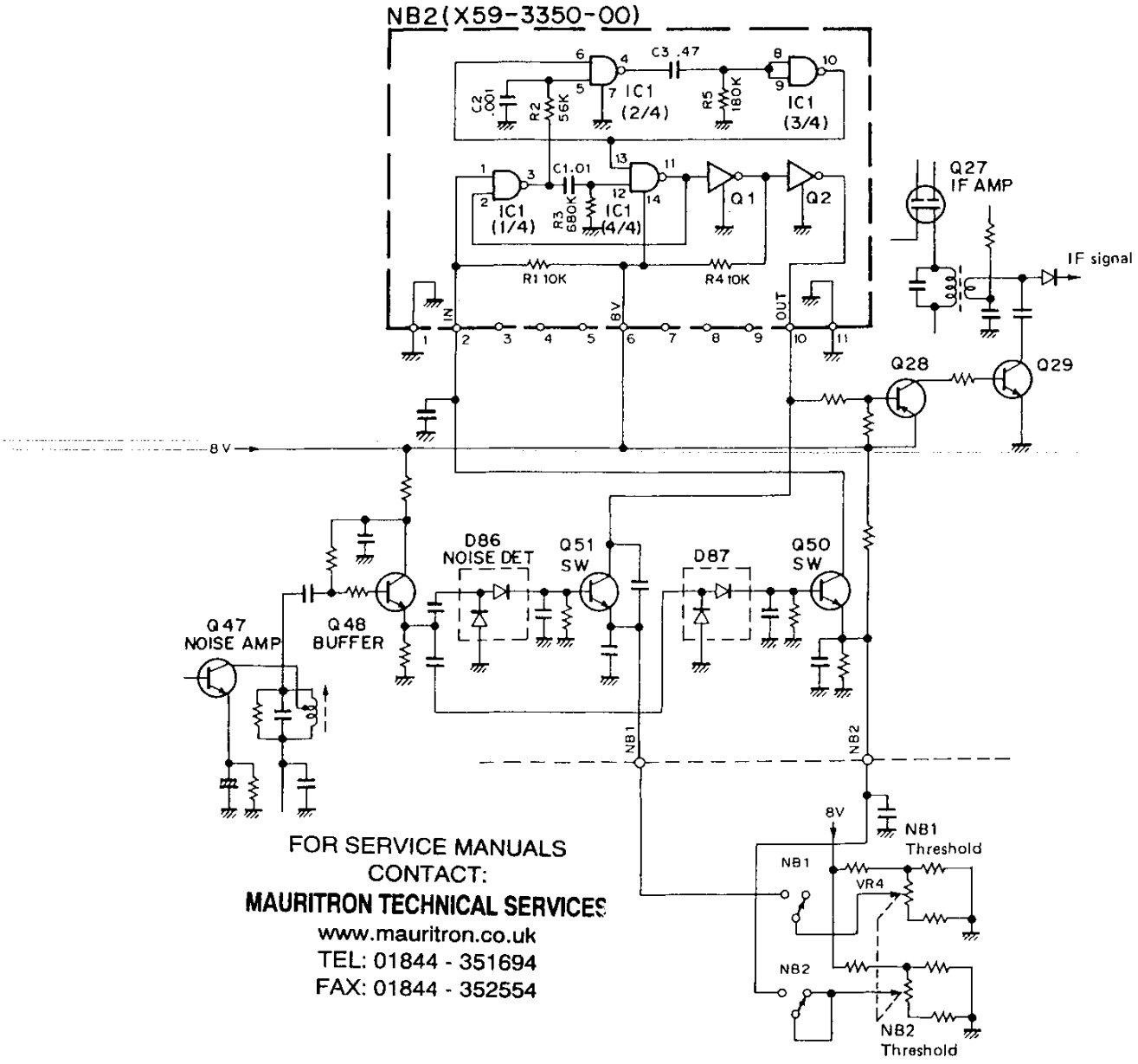


Fig. 4 Noise blanker circuit

CIRCUIT DESCRIPTION

Transmit Circuit Configuration

The transmit system operates utilizing double conversion for SSB, CW and AM and single conversion when operating in the FM mode.

The audio signal from the microphone terminal enters from the switch unit (CN5 "MIC"), and divides into a modulation and a VOX signal. The moduration signal is amplified by approximatery 20dB by IC1. Signals from data communications devices enter the ACC2 terminal on the rear panel of the radio and are applied to IC1. The output from IC1 is applied directly to the MIC GAIN cotrol on the front panel and to the FM modulation circuit.

The VOX signal is amplified by Q6 and enters the signal unit (CN501 "VOX"), and then enters the VOX module (X59-1080-00). The output from this module passes through the VOX switch and enters the DELAY TIME module (X59-3360-00) to cotrol the transmitter and receiver.

During SSB and AM operation the signal that passes through the microphone gain cotrol will enter the signal unit (CN1 "MV2"), where it is amplified by Q74 (2SC2712 Y) and applied to the balanced modulator IC3 (AN612). In the AM mode, however, the balance of IC3 is upset to generate the AM signal. Q74 does not operate in FM and CW modes because the voltage is applied to the emitter thru diode D89. The 455kHz DSB (Double Side Band) signal generated by IC3 passes through the transmit switching diodes D55 and D64, filter switching diodes D56, D57 (SSB), or D57, D60 (AM) to generate the 455kHz SSB or AM signal.

The SSB and AM signals pass through transmit switching diode D55, and are amplified by IF amplifier Q86. The carrier in CW mode optimizes the level past the PIN diode D74. The signal then passes through switching diodes D109, D110, and D122 and enters Q86 (3SK73GR).

Q86 is used to perform ALC (Automatic Level Control) and CW keying.

The 39.6MHz HET signal from the cotrol unit enters the signal unit (CN21 "HET") and is amplified by HET amplifier Q78 (3SK73GR). This HET signal passes through switching diode D100, in the SSB, CW and AM modes, and is fed into the first transmit mixer IC5.

The output from the IF amplifier also enters IC5 and is combined with the HET signal to generate a 40.055MHz signal.

The output from IC5 passes through a MCF, which removes spurious components and enters the second transmit mixer Q79 and Q80 (3SK122L).

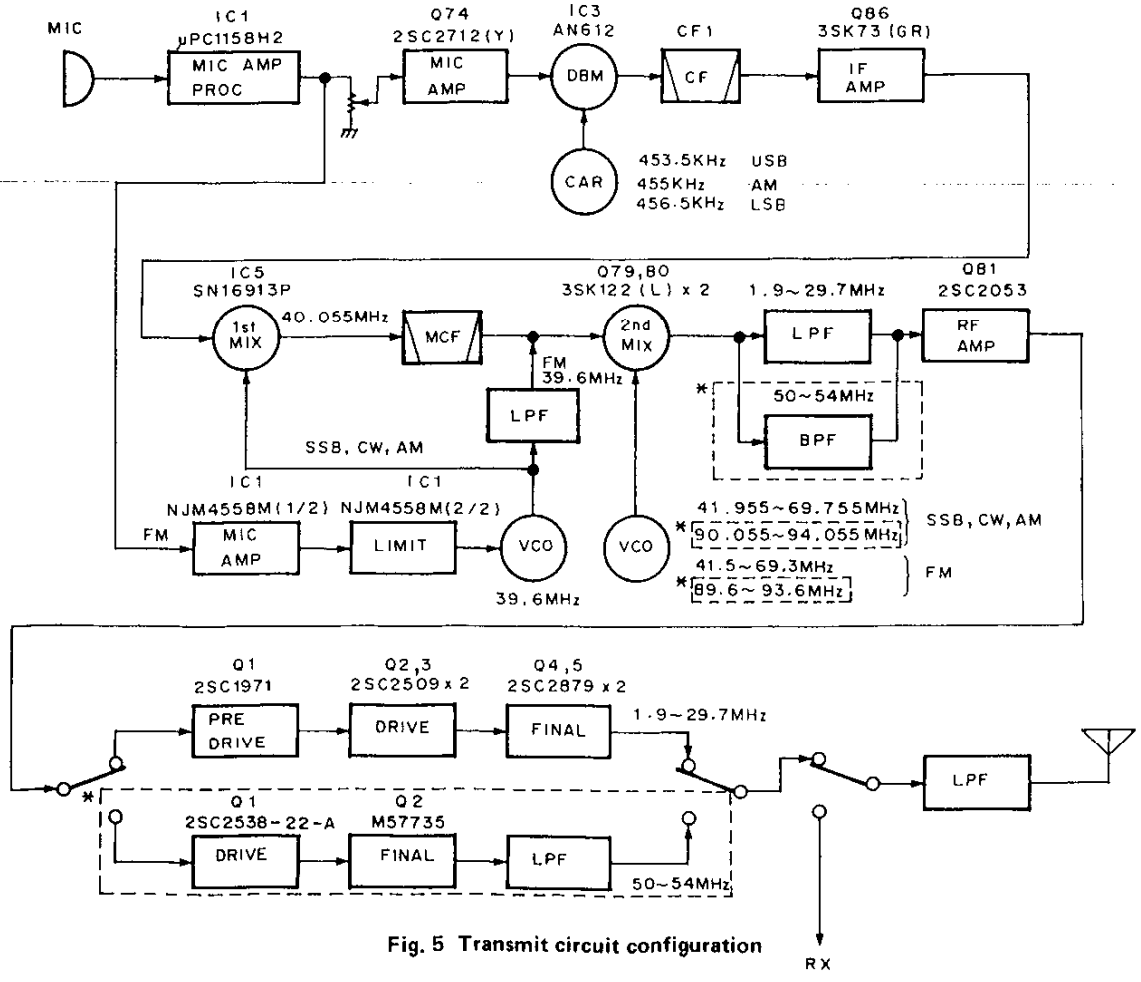


Fig. 5 Transmit circuit configuration

CIRCUIT DESCRIPTION

In FM the output of the MIC amplifier, IC1 of the switch unit, enters the signal unit FM MIC amplifier module (X59-3000-02). This module also functions as the MIC amplifier, limiter circuit, and low-pass filter circuit. The output enters the cotrol unit from the FMM terminal and modulates the 39.6MHz oscillator, VCO4. In modes other then FM, the power of the FM microphone amplifier module is not turned on, and therefore modulation is not affected.

The 39.6MHz signal from the control unit to the signal unit is the HET signal for SSB, AM, and CW modes and the first IF frequency in the FM mode. The IF frequency which enters the signal unit is amplified by IF amplifier Q78. Q78 is the ALC cotroller. The second gate of Q78 has a fixed bias in modes other then FM, therefore ALC does not fuction.

The output from Q78 (3SK73GR) passes through switching diodes D101, D102, and D124, a low-pass filter, and is delivered to the final mixer (the second mixer in modes other then FM). Since the IF frequency in the FM mode is different from that in the other modes, the frequency is corrected by the final VCO.

The signal is converted into an actual transmit frequency by the final mixer and passes through the IF trap (40.055 MHz) and low pass filter, is amplified by RF amplifier Q81, and passes through output transformer L111 to become the driver output.

The driver output from the signal unit now enters the final unit.

The output is amplified by final unit transistors Q1, Q2, Q3, Q4 and Q5 to generate a 100W final output. Then enters the filter unit.

The final unit output passes through the transmit/receive switching relay, K16, and individual low-pass filters for each band, and is then applied to the antenna terminal.

The ALC is detected by the output section of the low pass filter.

*The 50MHz band signal is separate from the HF band signal after it passes through the IF trap. This signal for the 50MHz band passes through switching diodes D104, and D106 and a band-pass filter. It is then amplified by RF amplifier Q81 (2SC2053), which is shared by the HF bands. Then the signal passes through the output transformer L11, enters the final unit, and is split from the HF path by relay K1. The signal is then applied to the filter unit. This signal is amplified to the required level by the drive amplifier (Q1) and power module Q2. It passes through the low pass filter, and is supplied to the antenna.

Standby Control Circuit

To switch between transmit and receive for full break-in, or for AMTOR/Packet use, the microprocessor sends various timing signals to control the transmit/receive circuits.

When the standby signal SS from the Standby switch is applied to the microprocessor, three signals are generated, CTX, RB, and CKY. Signals TXB, RXB, and RL are generated based upon these signals to operate the transmit/receive circuit.

The role of each of these signals is describe below:

SS: Reference signal to cotrol each signal (stadby switch, PTT switch, and key input)
CTX: Cotrol signal from the microprocessor to generate TXB
RB: Control signal to mute the receive signal line
CKY: Control signal for keying
TXB: 8V line for the transmit circuits
RXB: 8V line for the receive circuits
RL: 13.8V line for the transmit circuits
CKB: 8V line for keying generated by CKY

The signal timings are shown in the figure 6.

The timing after the standby switch is switched to transmit and until the system return to the receive state is as follows:

1. When SS goes low, the microprocessor judges whether the frequency is trasmittable or not. If so, the microprocessor switches CTX high 10ms after SS goes low.
2. Module unit (X59-3340-00) receive the CTX signal, and causes TXB and RL to go high.
3. CKY goes high 2ms after TXB goes high, CKB is driven to generate the keying voltage.
4. The transmit signal is emitted approximately 7ms after the CKB is actuated.
5. To return to receive, the transmit signal stops approximately 7ms after the SS line goes high, and TXB and RL return low, as RXB goes high.
6. The RB voltage used for turning on the receive signal line goes high 12ms after RXB goes high, and a signal is received.

CIRCUIT DESCRIPTION

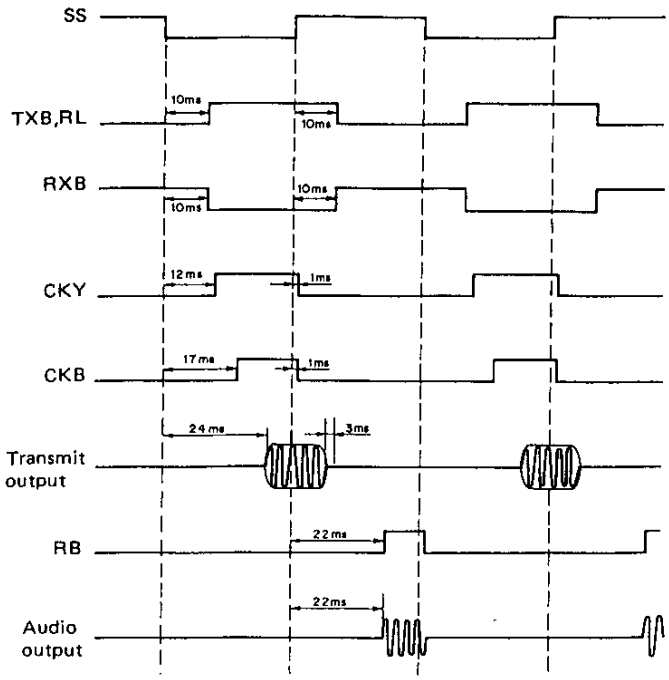


Fig. 6 Transmit/Receive timing chart

Break-in Operation

Manual keying

When the standby switch is turned ON, the base of Q90 (2SA1162Y) goes low, and Q91 (DTC114EK) turns on. CSS goes low, and CTX from the microprocessor turns on Q4 (DTC114EK) of the module unit (X59-3340-00). RL is emitted from Q1 (2SA1204Y), and TXB is applied from Q2 (2SA1204Y). Microprocessor output CKY turns on Q5 (DTC114EK) of the module unit (X59-3360-00), causing the emitter of Q7 (DTC114TK) to go to ground. One end of the Q7 collector is connected to Q87 (2SA1162Y) of the signal unit (X57-3190-00), and the other is connected to the key jack from Q84 (DTC114EK) from the COM terminal via the break-in changeover switch.

Q87 (2SA1162Y) is turned on and produce the CKB voltage when the key is closed, and Q86 (3SK73GR) of the send IF amplifier is keyed.

Semi-Break-In Keying

CW8 is applied to the base of Q84 and Q99. Therefore, they are ready to turn on when the emitter is connected to ground.

When the key is closed, the SEM terminal of the module unit (X59-3360-00) is connected to ground through Q99 and Q84 keys.

Q6 and Q2 in the module unit turn on, and trigger one-shot multivibrator IC1 (MB74LS122). A pulse is output from pin 8 to turn Q1 on and connect the SS line to ground.

When the key is closed, the IC8 output pulse returns to a low level and the SS line goes high after a time constant determined by setting of the VOX delay control VR7 and C254.

The key line switches Q87 via the COM terminal at this same time, and keys Q86 in real time.

Full Break-In

The key cunnects to the SS line and has the same function as the standby switch. When the key is closed, Q84 turns on, the base of Q90 is connected to the ground, Q91 is turned on, and CSS is switched low. The TXB and RL voltages are generated by the CTX signal, and the CKB voltage is used to generate the CKY signal voltage just as in manual keying.

Full break-in is different from manual keying in that the base of Q87 is controlled directly by the key in manual keying. In full break-in Q87 is controlled via Q5 and Q7 of the module unit (X59-3360-00) by the CKY signal from the microprocessor by turning the SS line on and off.

The reason is that in full break-in, the timing the transmit signal is set so that the radio signal is transmitted after the control signal is completely switched and the transmit system become stable; control is passed to receive after the signal stops, a receive signal is output, and the receive system becomes stable.

CIRCUIT DESCRIPTION

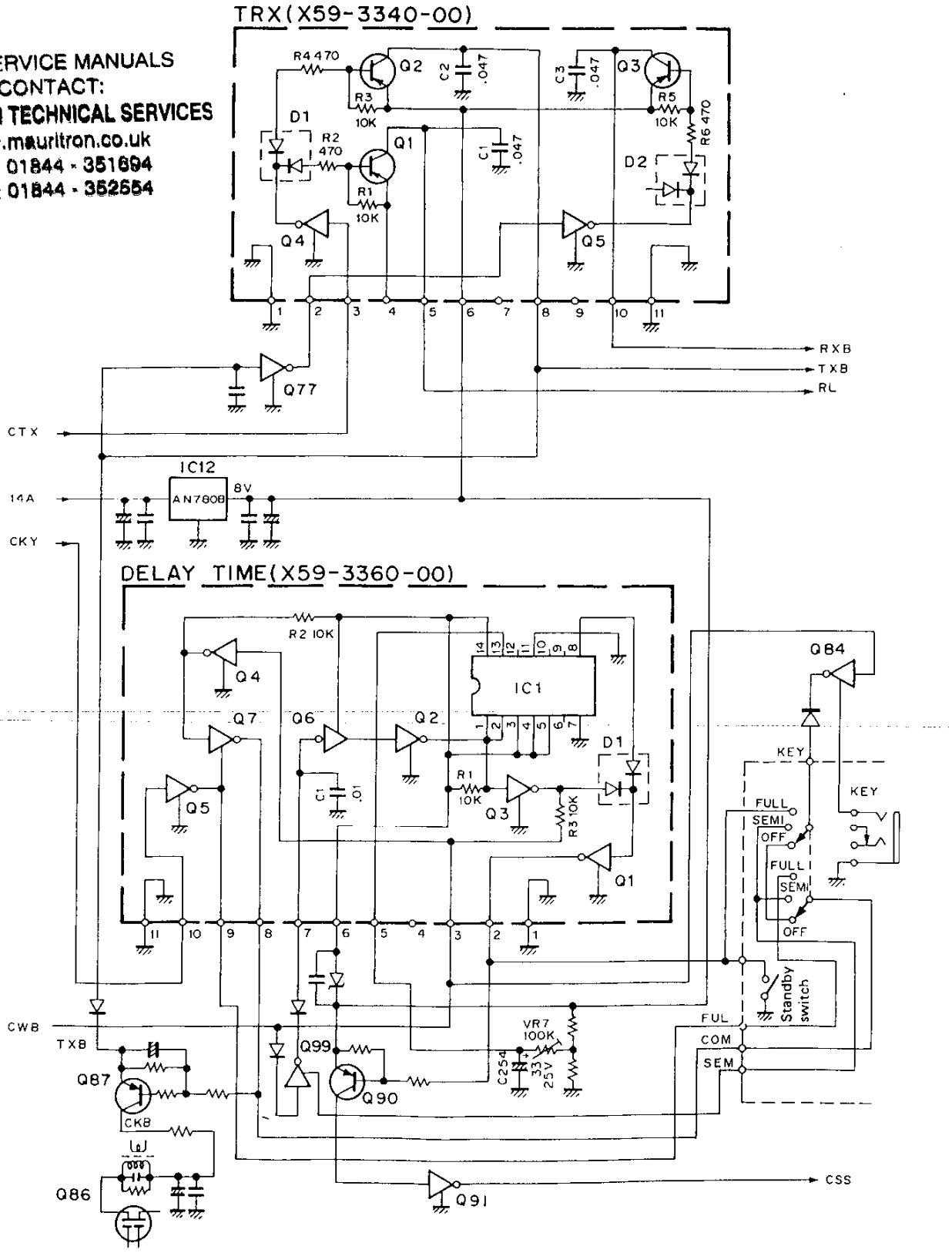


Fig. 7 Standby control circuit

CIRCUIT DESCRIPTION

ALC Circuit

A new ALC circuit is used to control the output according to the selected mode.

The output in the HF band is 100W for the CW mode, 110W for the SSB mode, and 50W for FM. therefore, the ALC detection voltage id defferent for each mode. CW is used and the standard reference mode. The gain of IC11 (3/4), in the ALC circuit, is varied according to the mode and transmit power. For example, since the output in FM is 50W the gain of IC11(3/4) must be increased by 3dB, with respect to the CW reference, to correct any deficiencies in the feedback voltage.

*Since the 50MHz band has only 10 watts output the gain of IC11(3/4) is increased by 10dB.

IC11(1/4) cotrols the ALC and power. IC11(1/4) functions as a differential amplifier in which the signal from IC11(3/4) enters the negative terminal and the power control voltage enters the positive terminal. As the transmitter output increases, the voltage at the negative terminal increases, and the output from IC11(1/4) decreases. When this output falls below the ALC reference of 2.5V, ALC action will begin.

The power is cotrolled by changing the voltage at the positive terminal of IC11(1/4). For the AM and CW modes the power is fixed at its maximum full power state since the center of VR2 (PC2) is held open.

The power cotrol voltage (PCV) changes with power, voltage and temperature. When the power, or voltage rises, the PCV is limited by zener diode D116 to avoid excessive power output. When the voltage falls, the power is increased. As the temperature rises, the resistance of thermister TH4 decreases, and the PCV rises, but excessive power output is prevented by the (negative) temperature coefficient of the zener diode. When the temperature falls, the PCV is reduced by the thermister, and power is reduced.

The drive level is also controlled in the FM mode. The input to IF amplifier Q78 (HET amplifier in modes other then FM) is controlled by PIN diode D96. The capacitor connected in parallel is provided to gain the minimum drive level at the maximum power.

VSWR Protection Circuit

To determine a time constant for the reflected wave, the reflected wave voltage is amplified by IC11(2/4) and applied to IC11(3/4) to provide protection.

Temperature Protection Circuit

The temperature detection circuit of the final unit is made modular to reduce its size. The surface temperature of the radiator is as follows:

Cooling fan start ..... 50 deg C
Cooling fan stop ..... 45 deg C
Temperature protection start ..... 80 deg C
Temperature protection stop ..... 70 deg C

When the temperature protection operates the ALC voltage and the power fall. The system does not return to the receive state.

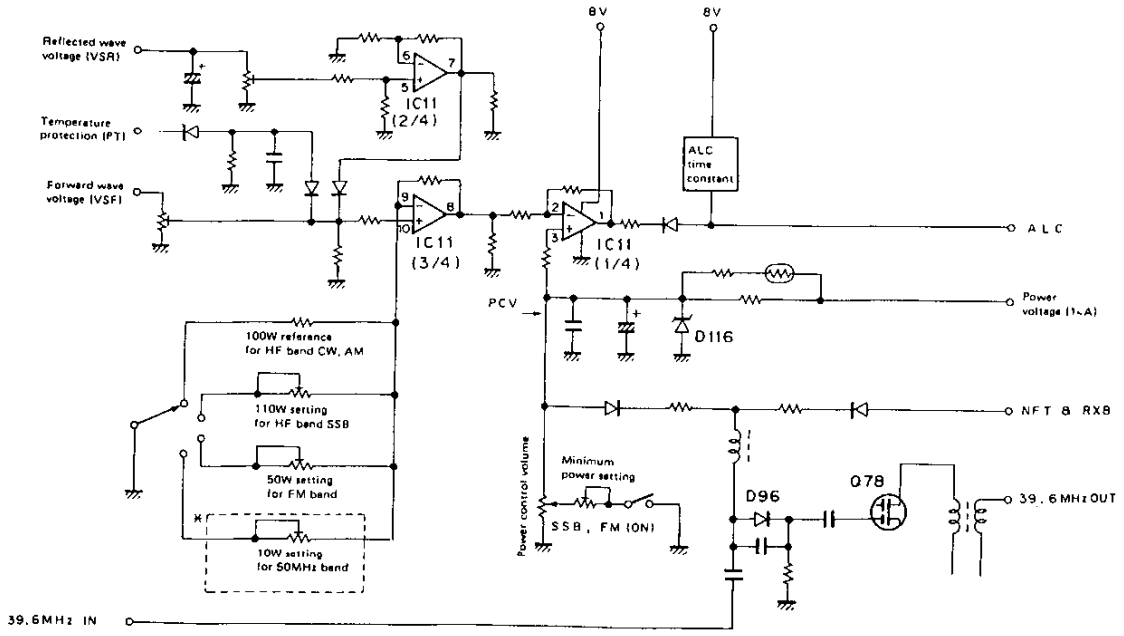


Fig. 8 ALC and power control circuit

CIRCUIT DESCRIPTION

Speech Processor Circuit

The SWITCH UNIT (A/4) IC1 is an audio type speech processor which also function as the first stage microphone amplifier. When the processor switch is OFF, the switch unit operates as a 20dB microphone amplifier. When the processor switch is ON, it operates as an ALC cotrolled amplifier with ALC with a maximum gain of 40dB.

The compression is set to approximately 20dB when the input signal to the MIC terminal is 10mV.

When the processor switch is ON, 8V DC is applie the base of the gain adjustment switching transistor Simultaneously the feedback amplifier begins operating.

When the switch unit is put on stand-by remotely data from terminal units connected to accessory term number 2 (such as packet, and AMTOR) Q2, Q3, and are turned ON, the microphone circuit is muted, the terminal is switched low, thus stabalizing the transmissio

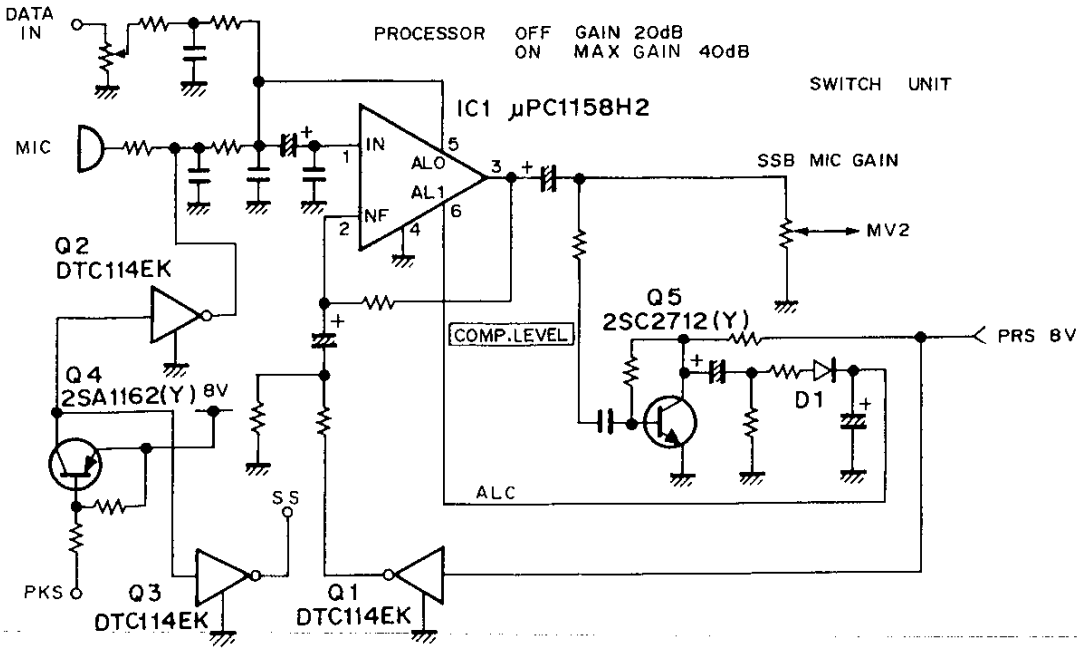


Fig. 9 Speech processor circuit

PLL Circuit

The TS-140 PLL circuit consists of three PLL loops which cover 500kHz to 30MHz in 10Hz steps with a reference frequency of 36MHz.

*The PLL circuit consists of four PLL loops, including 50MHz to 54MHz.

The carrier frequency is inserted into the PLL loop to provide the IF shift function. The carrier circuit PLL loop and the HET circuit PLL loop that aiways generates a 39.6 MHz frequency are also included. Division ratio data to these PLL loops cotrolled by the microprocessor. A single crystal frequency management method, in which phases are compared with that of a reference frequency fSTD, is used for this transceiver.

The block diagram of the PLL circuit is provided in figure 10.

The reference frequency fSTD, which is used as a basis for TS-140 frequency cotrol, is generated by a 36MHz crystal and oscillator Q9 (2SC2787L). The fSTD passes through buffers Q10 and Q12 (2SC2668Y), enters IC10 (SN16913P), passes through a LPF, and enters IC11 (SN16913P). This signal passes through buffer Q11 (2SC2668Y), and is divided by 8 in IC8 (M74LS93P) to generate a 4.5MHz signal. This signal passes through a LPF, and enters IC9 and IC11 (SN16913P) in the main loop. The signal passes through a LPF, and become the 4.5MHz reference frequency, fR, for each PLL circuit.

CIRCUIT DESCRIPTION

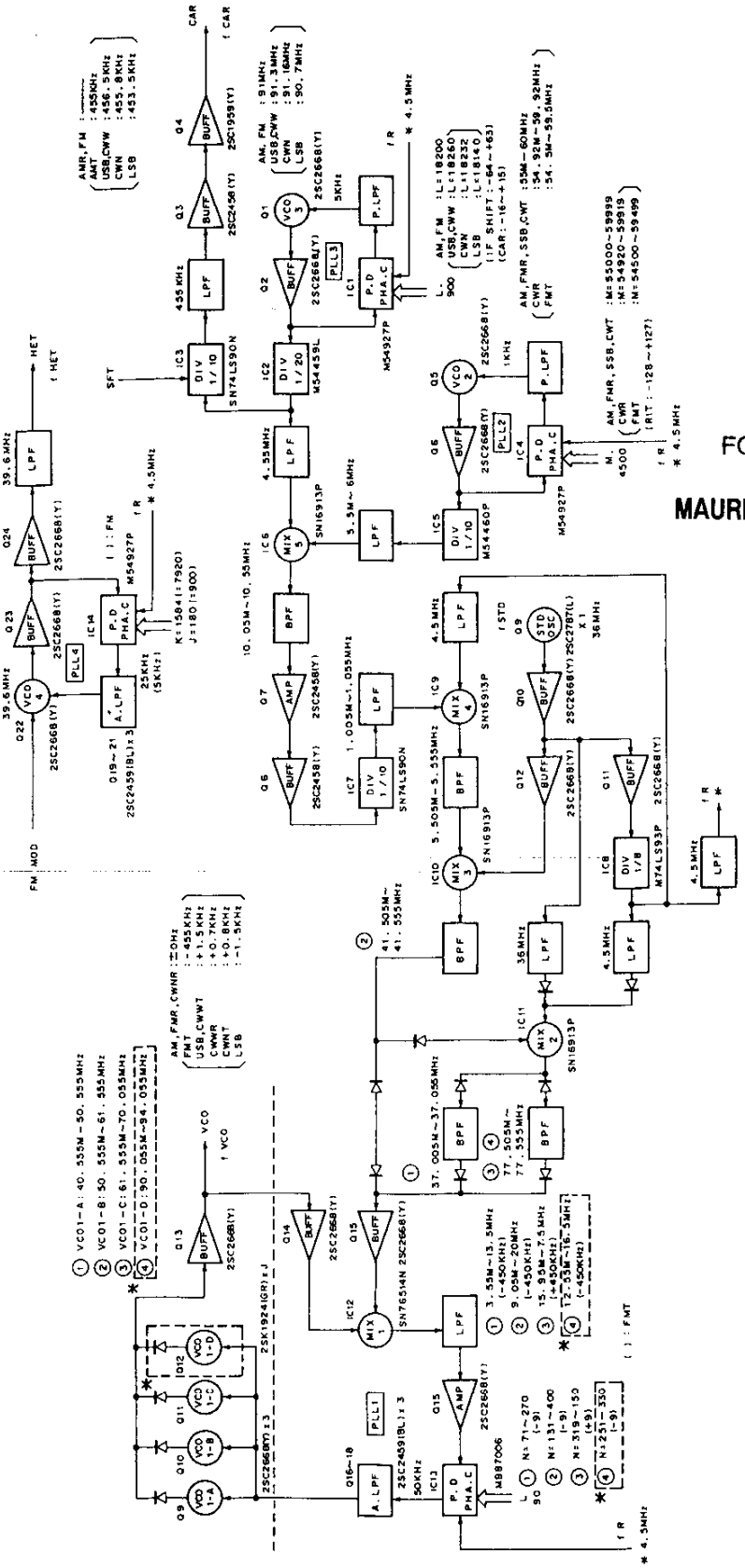


Fig. 10 PLL block diagram

CIRCUIT DESCRIPTION

PLL4

PLL4 consists of IC14 (M54927P), and VCO4, Q22 (2SC2668Y), is locked at 39.6MHz. The 4.5MHz reference frequency, fR, is applied to IC14 pin 15, and is divided internally by 180 (900 for FM) to generate a comparison frequency of 25kHz (5kHz for FM). The from VCO4 output passes through buffer Q23(2SC2668Y), applied to IC14 pin 3, and divided internally by 1584 (7920 for FM). The resulting signal is compared with the 25kHz (5kHz for FM) reference signal by the phase comparator, thus locking VCO4. Division ratios K and J are transmitted from digital control circuit via DA, CK, and PR4.

The output from PLL4 passes through Q24 (2SC2668Y) and a LPF and is fed into the signal unit as the HET signal.

PLL3

PLL3 consists of IC1 (M54927P), and VCO3, Q1 (2SC 2668Y), is locked at about 91MHz with a frequency that varies with the mode.

The 4.5MHz reference frequency, fR, is applied to IC1 pin 15, and divided internally by 900 to generate a 5kHz comparison frequency. The output from VCO3 passes through buffer Q2 (2SC2668Y), is applied to IC1 pin 3, and multiplied internally by the division ratio (about 1/18200) determined according to the mode. The resulting signal is compared with the 5kHz reference signal by the phase comparator, thus locking VCO3. Division ratio L is transmitted from the digital control circuit via DA, CK, and PR3.

The PLL3 output is divided by 20 in IC2 (M54459L), and directed to two circuits. One signal enters IC3 (SN74 LS90N) of the carrier circuit, is divided by 10, passes through a LPF, buffers, Q3 (2SC2458Y) and Q4 (2SC 1959Y) and fed into the signal unit as a carrier signal. During AM reception and AM/FM transmission, IC3 operation is stopped by the SFT data signal to remove the carrier signal.

The other signal is divided by 20, passes through a LPF, and enters MIX5 IC6 (SN16913P) in the main loop, which is part of the digital VFO. Therefore, the operating frequency remains unchanged even if the carrier frequency is changed to implement features, such as USB/LSB mode switching, IF shift, and fine adjustment of the carrier point. IF shift allows a shft of ±1kHz or more during SSB and CW receive The carrier point can be finely adjusted, in the SSB mode, thru a range of −400Hz to +375Hz.

PLL2

PLL2 consists of IC4 (M54927P), and VCO2, Q5(2SC 2668Y), is locked thru a range of 55MHz to 59.999MHz, except in CW receive and FM transmit. The 4.5MHz reference frequency, fR, is applied to IC4 pin 15, and divided internally by 4500 to generate a 1kHz comparison frequency. The from VCO2 output passes through buffer Q6 (2SC2688Y), is applied to IC4 pin 3, and divided internally by M. The resulting signal is compared with the 1kHz reference signal, by the phase comparator, thus locking VCO2. Division ratio, M, is transmitted from the digital control circuit as division data in 4,999 steps (55,000 to 59,999) corresponding to the range of 0.00kHz to 49.99kHz or 50.00 kHz to 99.99kHz via DA, CK,, and PR2.

Correction is performed according to the mode and RIT operation. To obtain the 800Hz beat tone obtained during CW reception, M is shifted (54,920 to 59,919) by about 80. Since the VCO1 output frequency during FM transmit is 455kHz lower than thatduring receive, it is corrected 5kHz (54,500 to 59,499) by VCO2. (450kHz is corrected by PLL1.) When the RIT is operating, the M division ratio is varied so that the from VCO1 output frequency is shifted ±1.2kHz or more.

In AM and FM modes, the frequency is shifted 10 steps, and operates in 100Hz steps as shown in the frequency display.

The PLL2 output is divided by 10 in IC5 (M54460L), passes through a LPF, and is applied to pin 2 of MIX5 IC6 (SN16913P). The signal is mixed with the signal generated by PLL3, passes through a BPF, and become a signal of 10.05MHz to 10.5499MHz, in 100Hz steps. The signal passesthrough amplifier Q7 (2SC2458Y), buffer Q8 (2SC 2458Y), is divided by 10 in IC7 (SN74LS90N), passes thru a LPF, and is applied to pin 2 of MIX5 IC9 (SN16913P). The signal is mixed with the 4.5MHz signal generated by dividing the reference frequency by 8 in MIX4 (SN16913P), passes through a BPF, become a signal of 5.505MHz to 5.55499MHz in 10Hz steps, and is applied to pin 2 of MIX3 IC10 (SN16913P). In addition, the signal is mixed with the 36MHz reference frequency by MIX3, passes through a BPF, and become a signal of 41.505MHz to 41.50499MHz.

CIRCUIT DESCRIPTION

PLL1

The final PLL1 loop consists primarily of IC13 (MB 87006). The final VCO1 is located in the signal unit, and consists of three VCOs, VCO1A to VCO1C, that cover a dial frequency of 500kHz to 30MHz. (*The final VCO1 consists of four VCOs, VCO1A to VCO1D, in the range of 50MHz to 54MHz.) Any of the VCOs can be selected according to band information from the digital cotrol circuit. The VCO1 signal passes through buffer Q13 (2SC2688Y) of the signal unit, and is applied to the PLL circuit of the control unit. This signal passes through buffer Q14 (2SC 2668Y), and is applied to pin 5 of MIX1 IC12 (SN76514N). The signal is mixed with the signals generated by PLL3 and PLL2. This input signal is also divided into three signals according to band information.

One of the signals generated in the previous loop is applied directly to buffer Q13 (2SC2668Y) by the diode switch according to the band information. The other signal is applied to pin 2 of MIX2 IC11 (SN16913P). When the operating frequency is 500kHz to 10.5MHz, the signal is mixed with the 4.5MHz signal generated by dividing the reference signal by 8 in MIX2, passes through a BPF, become a signal of 37.005MHz to 37.05499MHz, and is applied to buffer Q13. When the operating frequency is 10.5 MHz to 21.5 MHz, the signal is applied directly to buffer Q13 without passing through MIX2. When the operating frequency is 21.5MHz to 30MHz, the signal is mixed with the reference frequency in MIX2, passes through a BPF, becomes a signal of 77.505MHz to 77.55499MHz, and is applied to buffer Q13.

*When the operating frequency is 50MHz to 54MHz, the signal is processed in the same way as the signal for 21.5MHz to 30MHz.

These signsls are applied to pin 11 of MIX1 IC12 through buffer Q13. The difference signal passes through a LPF to become a signal of 3.55MHz to 20MHz, passes through amplifier Q15 (2SC2668Y), and is applied to pin 8 of PLL IC13.

The 4.5MHz reference frequency, fR, is applied to IC13 pin 1, and divided internally by 90 to generate a 50kHz comparison frequency. The signal input to IC13 is divided by N, and compared with the 50kHz reference signal, by the phase comparator. The signal psses through an active LPF, Q16 to Q18 (2SC2459BL), and is sent to the signal unit as the VCO voltage, to control the varactor diode of the last VCO1.

Division ratio, N, covers the overall operating frequency range in 50kHz steps, exept during FM transmit. During FM transmit, N is shifted 9 steps (450kHz) so that the VCO1 output frequency becomes −455kHz. The division ratio is sent from the digital control circuit via DA, CK, and PR1.

Therefore, the final output of PLL1 is 40.555MHz to 70.05499MHz (shifted by −455kHz for FM transmission) as determined by the values of L, M, and N, in 10Hz steps.

*The final output of PLL is 40.555MHz to 70.05499 MHz or 90.055MHz to 94.05499MHz in 10Hz steps.

UNLOCK Detection

If any PLL loop becomes unlocked, pin 11 of IC1, IC4, IC14 and/or pin 7 of IC13 go low, and act as an OR circuit. These signals pass through switching transistors Q25 (DTA 124ES) and Q26 (DTA124ES), and the "L" is sent to the digital cotrol circuit.

At this point, the microprocessor will display the unlock status, and emits the SBK signal to stop the IF signal before the filter via Q29 (2SC2712Y), and the MUTE signal for stopping the audio signal via Q57 (2SC2712Y) before entering the volume control.

50kHz Marker Signal

IC13's 50kHz comparison frequency is emitted from pin 13 and used as a marker signal.

CIRCUIT DESCRIPTION

Digital Control Circuit

Configuration of microprocessor peripheral circuits

As shown in figure 11, the units around microprocessor IC18 (BU18400A) include 16K ROM, IC21 (MBM27C128-25JAJ2), 2K static RAM, IC20 (TC5518CPL), extended I/O IC (TMP8255AP-5; IC22 and IC23 for output only, and IC24 for input only), encorder processing gate array IC26 (LZ92K37), and the microprocessor optional IF-IOC communication IC (μPD8251AFC). The microprocessor address signal is selected by transmitting the chip select signal from IC19 (SN74LS138N). IC15 (PST520D) generates a reset signal according to changes in the 5V line, to reset the microprocessor, the extended I/O IC, and communications IC. The reset signal is also sent to RAM to prevent data destruction due to shock noise when switching power on and off. IC16 (TC4069UBP) rectifies the waveform of the reset signal, and also functions as the buzzer oscillator circuit and system clock oscillator circuit. The timer IC, IC17 (NE555C), generates an AC signal for dynamic lighting of the fluorescent display tube, and gives an interupt signal to the microprocessor. The dynamic lighting function is controlled by the microprocessor. The μPC6300C is the fluorescent display tube driver IC. IC27 (MB4052) is an A/D converter IC to which a voltage corresponding to the rotational position is applied by a variable resistor such as the RIT. IC25 (TC4069UBP) operates as a chatter absorption circuit for the mechanical-type sub-dial rotary encorder.

Most of these circuit are located in the control unit, but the fluorescent display tube, drive IC (μPD6300C), and voltage generation DC/DC module (CPS1175B) are in the display unit.

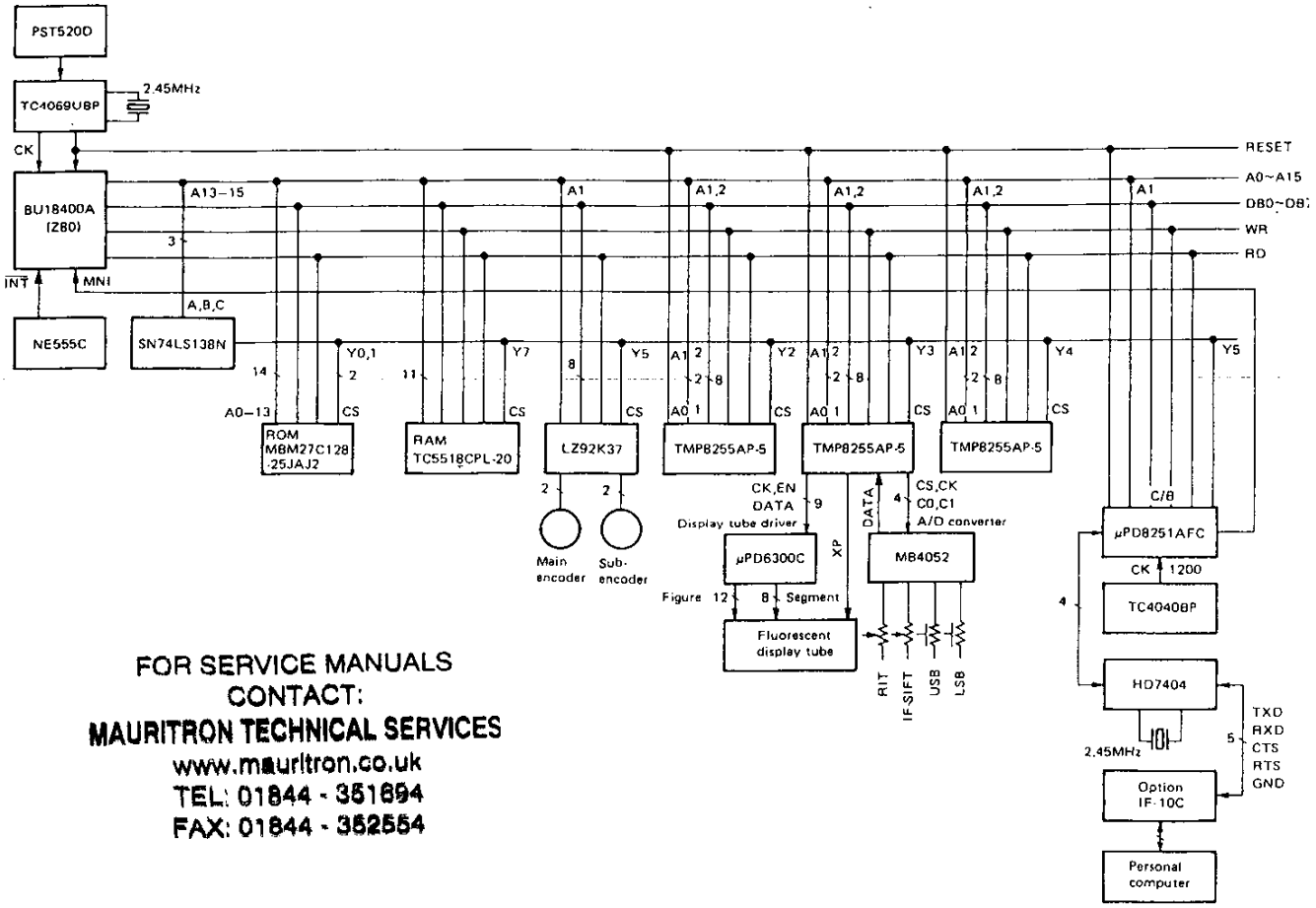


Fig. 11 CPU peripheral circuit

CIRCUIT DESCRIPTION

System Clock Oscillation and System Reset Circuit

Microprocessor IC18 (BU18400A) requires a 2.45MHz system clock. Ceramic oscillator X2 and IC16 (TC4069 UBP) are used to generate the system clocks (figure 12).

IC15 (PST520D) is a reset IC which sends a reset signal to the microprocessor and I/O when the power supply voltage reaches about 4.3V, which halts all function immediately. When the power supply voltage exceeds aproximately 4.3V, the reset signal is emitted and after the time constant set by R151 and C219 elapses, the microprocessor is initialized and operation resumes (figure 13).

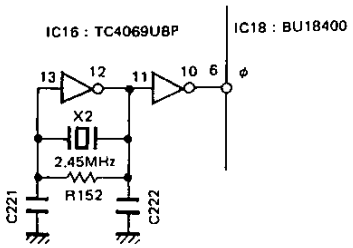
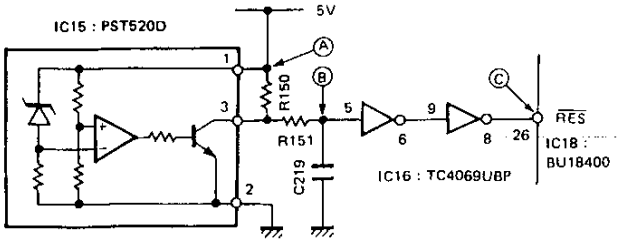


Fig. 12 System clock oscillation circuit



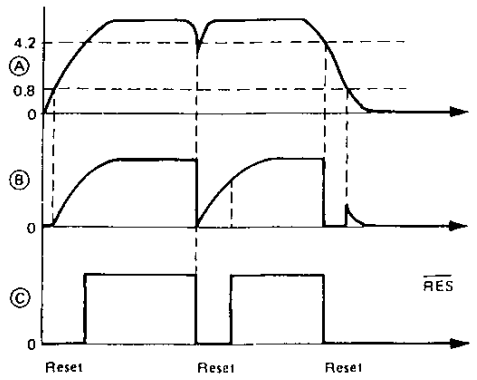
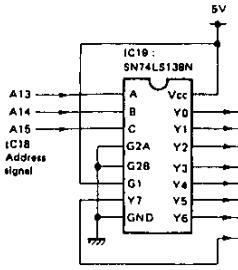


Fig. 13 Reset circuit

Address Control

Microprocessor address lines A0 to A15 cannot select ICs directly, so they are decoded into selection signals by IC19 (SN74LS138N). IC19 has a 64K-bytes memory area which is divided equally into 8 blocks (8K bytes each) and assigned to the ICs. Address control division is shown in figure 14.



Function	Destination	Physical address
ROM	IC21 ㉑	0000H – 1FFFH
ROM	IC21 ㉒	2000H – 3FFFH
I/O	IC22 ⑧	4000H – 5FFFH
I/O	IC23 ⑨	6000H – 7FFFH
I/O	IC24 ⑩	8000H – 9FFFH
Encoder gate array	IC26 ⑦	A000H – BFFFH
Serial I/O (option)	IC 1 ⑪	C000H – DFFFH
RAM	IC20 ⑫	E000H – FFFFH

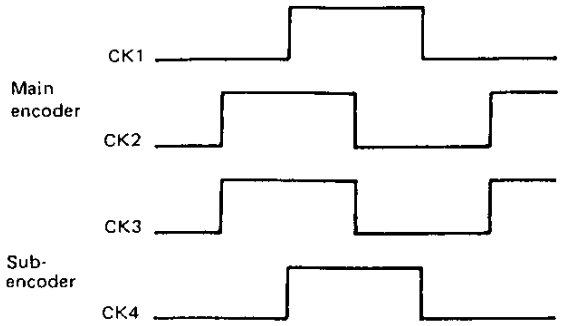
Fig. 14 Address control division

CIRCUIT DESCRITPION

Encorder Peripheral Circuit

IC26 (LZ92K37) detects the rotational direction from the dual-phase rotary encorder pulse input, counts up or down, and has two inputs. CK1 and CK2 count all leading and trailing pulse edges, and performs quadruple functions. CK3 and CK4 count the leading and trailing edges of CK3, and performs dual functions. The main dial is an optical type, which inputs signals directly. The sub-dial is a mechanical type, which inputs signals through the chatter absorption circuit.

Count data can be read in the same manner as when reading RAM. CK1 and CK2 have one counter, CK3 and CK4 have another counter. When IC26 A0 is low, the CK1 and CK2 data is read. When A0 is high, the CK3 and CK4 data is read.



CK1 to CK4 input terminals have built-in pullup resistors.

Fig. 16 Waveforms of IC26, CK1 to CK4, when the dial is turned clockwise

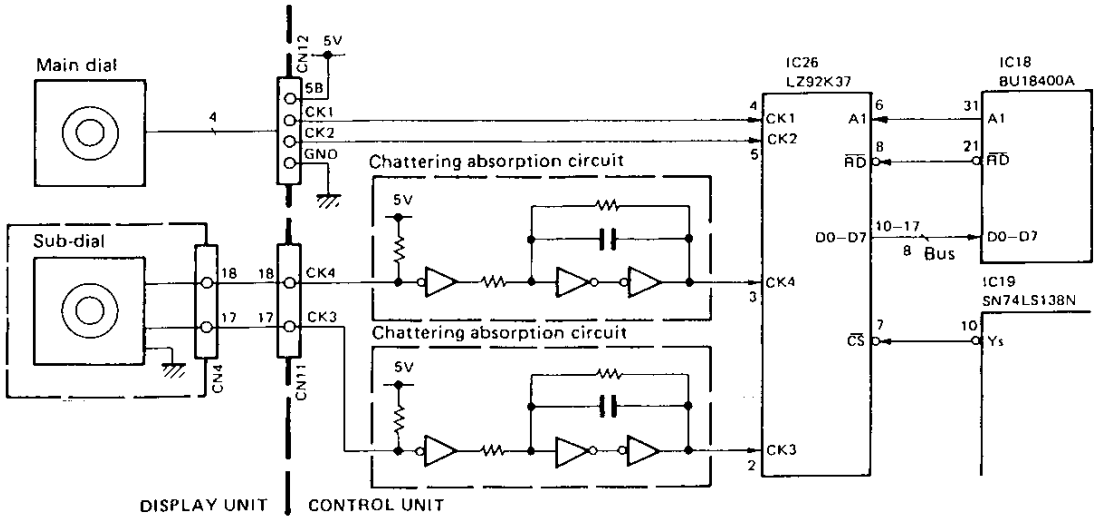


Fig. 15 Encoder peripheral circuit

Display Circuit

The fluorescent display tube is dynamically lit by IC18 (BU18400). The lighting period for one column is given by a negative pulse of IC17 (NE555C). When a low level is applied to the INT input, IC18 starts its interrupt procedure, outputs one column of display data, and the column signal to the fluorescent display tube driver MPD6300C through IC23 (TMP8255AP-5), and outputs data and control signal to the XP terminal, via IC22 port C7. Normally, one cycle ends when the data and signal are output 12 times, since there are 12 columns. However, for yellow (mode) display columns, the data and signal are output 3 times in one cycle because of a lack of sufficient intensity.

Display unit, T1, is the DC/DCE module which generates the drive voltage and filament voltage of the fluorescent display tube. The filament voltage waveform is generated by the oscillator circuit in that module. The frequency fluctuates because the column loads differ from each other, causing a variation in the oscillator frequency. The μPD 6300C input waveforms are seen in each of the oscillator periods of IC17 (See figure 18). Data is shown in figure 19. It is output from the left.

CIRCUIT DESCRIPTION

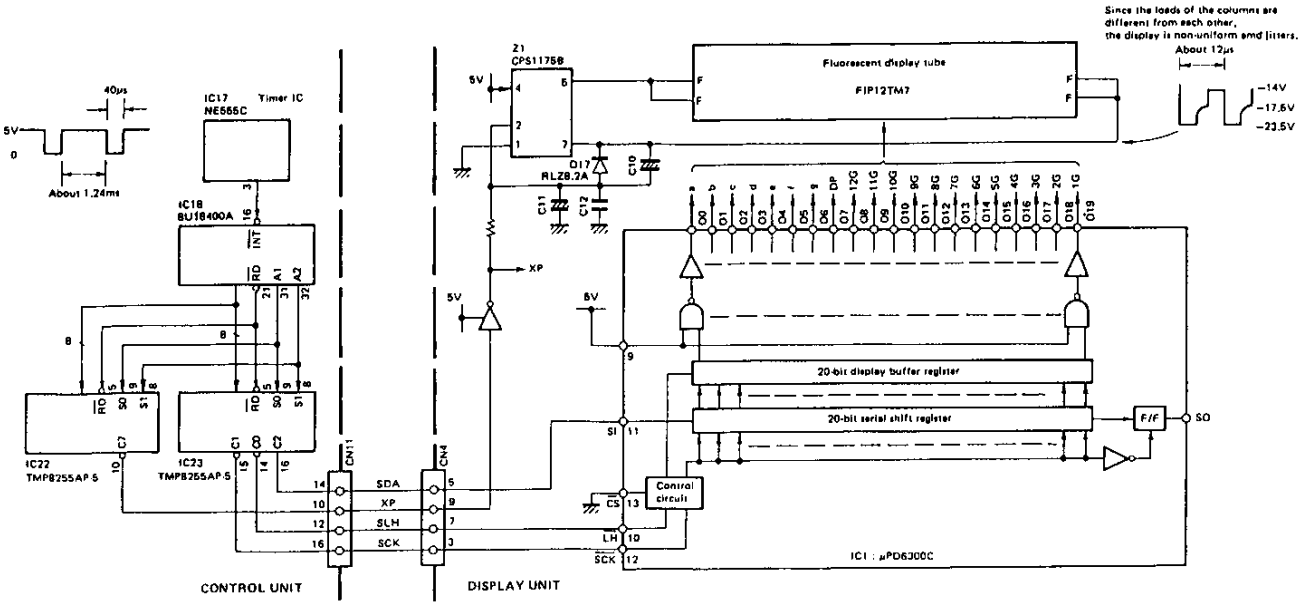


Fig. 17 Display circuit

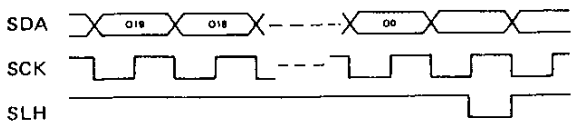


Fig. 18

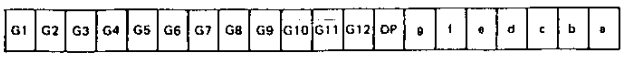


Fig. 19

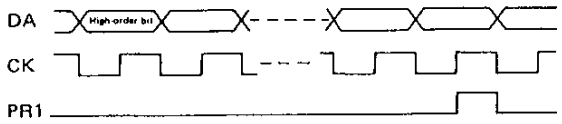


Fig. 20

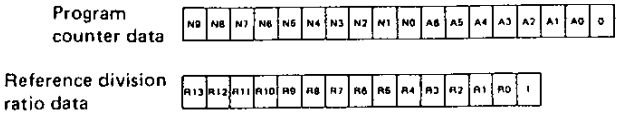


Fig. 21

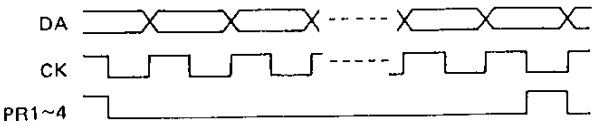


Fig. 22

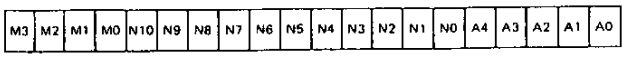


Fig. 23

PLL Data Output

Four PLLs are controlled. The 50kHz-step loop PLL1 uses the MB87006, and other loops use the M54927P.

Data is output for the MB87006 as shown in figure 20.

Both reference division ratio data and program counter data are given to the MB87006. Reference division ratio data are supplied only when the power is turned on. The data formats are as shown in figure 21. Data is output from the left.

Data is output to the M54927P as shown in figure 22.

Data output to the M54927P is shown in figure 23. It is output from the left.

This PLL data is output only to the PLL when changed.

CIRCUIT DESCRIPTION

Band Output

The BPF and LPF are switched by output ports A0 to A4 (B0 to B4) of IC22 (TMP8255AP-5). The PLLs are switched by output ports C4 to C6 (VB1 to VB3). The levels of the ports in each frequency range are shown in the figure below:

Freq' (MHz)	B4	B3	B2	B1	B0	VB3	VB2	VB1
0 – 0.5	H	L	L	L	L	L	L	H
0.5 – 1.6	H	L	L	L	H	L	L	H
1.6 – 2.5	L	L	L	H	L	L	L	H
2.5 – 4.0	L	L	L	H	H	L	L	H
4.0 – 6.5	H	L	H	L	L	L	L	H
6.5 – 7.5	L	L	H	L	H	L	L	H
7.5 – 10.5	H	L	H	H	L	L	L	H
10.5 – 14.5	L	L	H	H	H	L	H	L
14.5 – 19.0	H	H	L	L	L	L	L	L
19.0 – 21.5	L	H	L	L	L	L	L	L
21.5 – 25.0	H	H	L	L	H	H	L	L
25.0 – 30.0	L	H	L	L	H	H	L	L
50.0 – 54.0	L	H	L	H	L	H	L	L

Table 6

A/D Converter Analog Input

The four types of analog input, RIT, IF shift, carrie point correction for LSB and USB, are A/D converted, anc loaded into the microprocessor as digital values. The con trol unit has the A/D converter, IC27 (MB4052), to whicl a channel select signal (CS) and data input control signal (C0 and C1) are applied.

The microprocessor sends a channel select signal first then a positive pulse from the A2 port of IC23 (TMP825 AP-5) to reset the A/D coverter IC27 (MB4052). After 9 clock pulses have been sent from IC23 C6 port, the con verted digital values are sent from A/D converter IC27 tc the C6 port ofIC24: TMP8255AP-5 in synchronization witl the clock pulses. The A/D converter peripheral circuit anc timing charts are shown in figures 24 and 25.

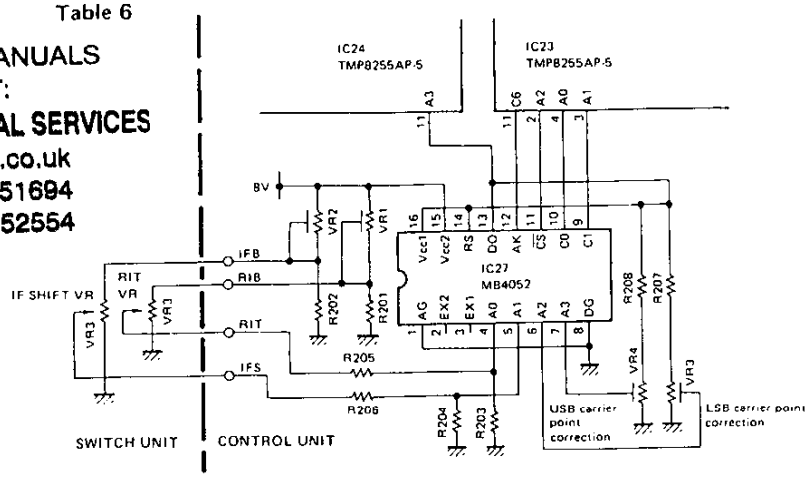


Fig. 24 A/D converter peripheral circuit

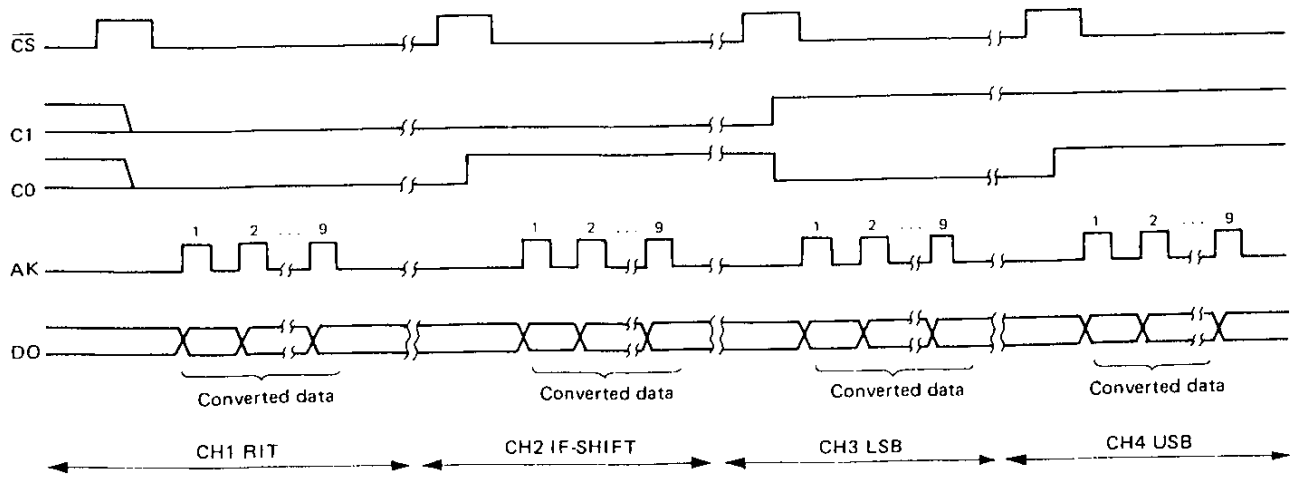


Fig. 25 A/D converter data read timing chart

CIRCUIT DESCRIPTION

Key Scan and Extended Diode

A key scan signal with a negative pulse is sent from ports B4 to B7 and C5 of IC23 (TMP8255AP-5). One column, corresponding to ports B0 to B3 of IC24 (TMP8255AP-5) is selected, and the ON/OFF state of the switch is sensed. When the switch at an intersection of the matrix is on, the corresponding bit of ports B0 to B3 of IC24 goes low, thus detecting. The activation of the switch.

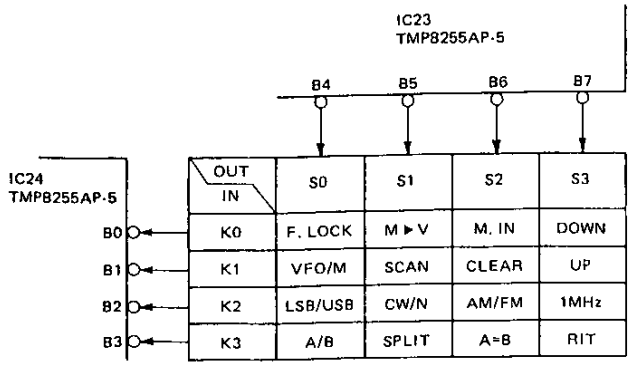


Fig. 26

Transmit Timing Control Signal

The full Break-in timing is generated by the microprocessor, and is sent as the CTX, RB, and CKY signals from port C of IC22 (TMP8255AP-5). When transmit/receive switching is detected at port A6 of IC24 (TMP8255AP-5), the CSS signal is output with the following timing.

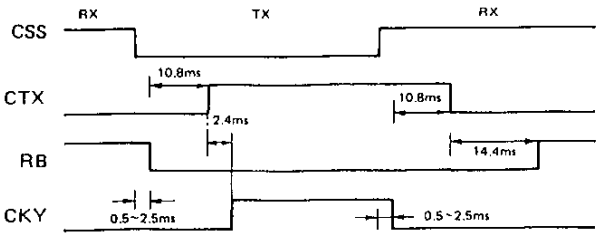


Fig. 27

SFT Output

The SFT output signal is output during FM and AM reception, and stops the CAR output.

TOB Output

The TOB output is stored in the memory channel, split channel, in FM mode, and output only during transmission. Repeater subtone control signal.

14V Input

To clear any meaningless display when the power switch is turned on or off, the 13.8V line is monitored. When this input goes low, the display is cleared.

SBK and MUT Output

This signal cuts the PLL switching noise.

I/O port functions

1) IC22 (Output only)

Terminal Name	Pin No.	Symbol	Function	Active level
A0	4	B0	Band switching output. (See the text.)	H
A1	3	B1		
A2	2	B2		
A3	1	B3		
A4	40	B4		
A5	39	50M	Unused.	H
A6	37	HFL		
A7	37	HFL		
B0	18	MUT	Cut the AF signal.	H
B1	19	PD	28MHz band power down.	H
B2	20	SBK	Cut the RF signal.	H
B3	21	CWN	Indicates CW-N.	H
B4	22	FM	Mode output.	H
B5	23	AM		
B6	24	CW		
B7	25	SSB		
C0	14	CTX	Transmit control signal. (See the text.)	H
C1	15	RB		
C2	16	CKY		
C3	17	TOB	Output the subtone (Option).	H
C4	13	PB0	PLL band switching signal. (See the text.)	H
C5	12	PB1		
C6	11	PB2		
C7	10	XP	Fluorescent display tube red letter segment signal.	L

CIRCUIT DESCRIPTION/SEMICONDUCTOR DATA

2) IC23 (Output only)

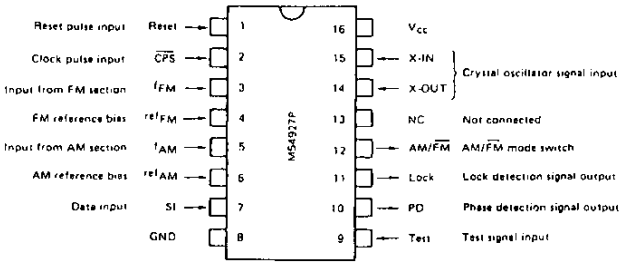
Terminal Name	Pin No.	Symbol	Function	Active level
A0	4	C0	IC27:MB4052 control signal. (See the text.)	
A1	3	C1		
A2	2	CS		
A3	1	SFT	CAR cut signal.	H
A4	40	PR1	PLL enable signal. (See the text.)	
A5	39	PR2		
A6	38	PR3		
A7	37	PR4		
B0	18	LF	F.LOCK LED signal.	H
B1	19	LM	M.SCR LED signal.	H
B2	20	L1	1MHz LED signal.	H
B3	21	–	Unused.	
B4	22	S0	Key scan output. (See the text.)	L
B5	23	S1		
B6	24	S2		
B7	25	S3		
C0	14	SLH	Fluoresent display tube drive IC signal. (See the text.)	
C1	15	SCK		
C2	16	SDA		
C3	17	EN	Unused.	
C4	13	DA	PLL data signal. (See the text.)	
C5	12	CK		
C6	11	AK	IC27:MB4052 control signal. (see the text.)	
C7	10	BZ	Turns the buzzer oscillator circuit on.	H

3) IC24 (Input only)

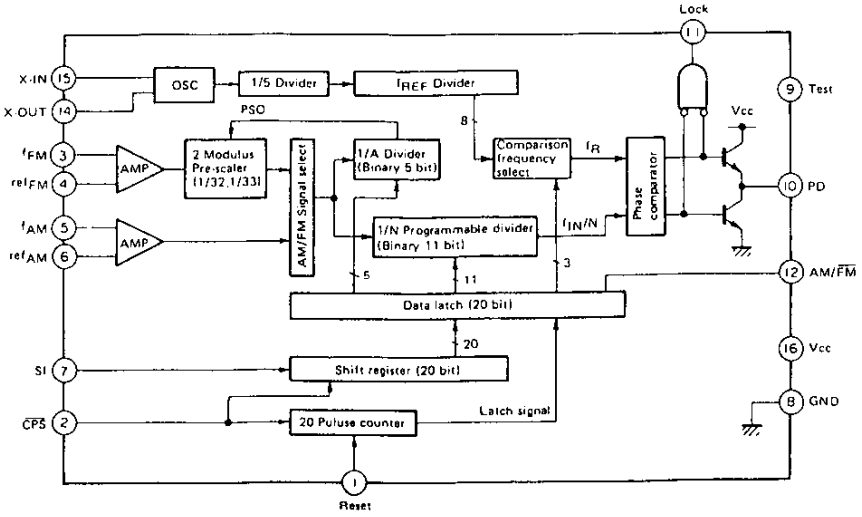
Terminal Name	Pin No.	Symbol	Function	Active level
A0	4	–	Unused.	
A1	3	–		
A2	2	UL	Detect the unlock state.	L
A3	1	AD	IC27:MB4052 data signal.	
A4	40	MU	MIC UP/DOWN switch.	L
A5	39	MD		
A6	38	CSS	CSS line signal transmission detection.	L
A7	37	14V	Power switch off detection.	L
B0	18	–	Unused.	
B1	19	–		
B2	20	–		
B3	21	–		
B4	22	–		
B5	23	–		
B6	24	–		
B7	25	–		
C0	14	–	Unused.	
C1	15	–		
C2	16	–		
C3	17	–		
C4	13	–		
C5	12	–		
C6	11	–		
C7	10	–		

M54927P : PLL IC (Control unit IC1, 4, 14)

- Terminal connection diagram



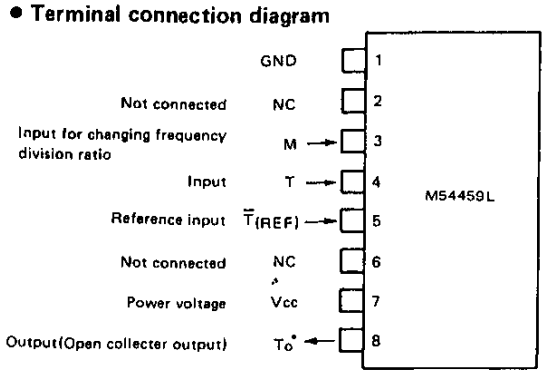
- Block diagram



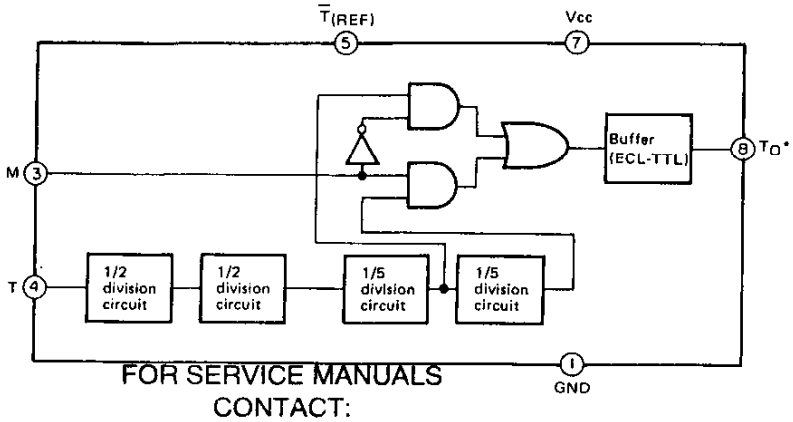
SEMICONDUCTOR DATA

M54459L : Divider (Control unit IC2)

- **Terminal connection diagram**



- **Block diagram**

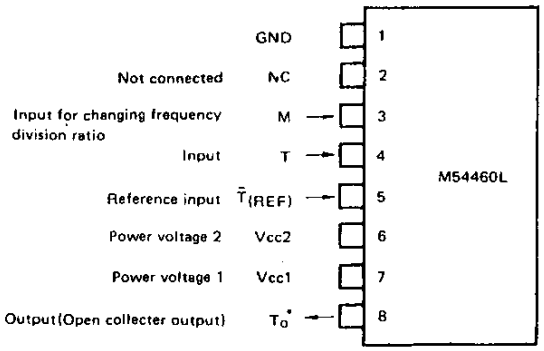


- **Input for changing frequency division ratio (M) and division ratio**

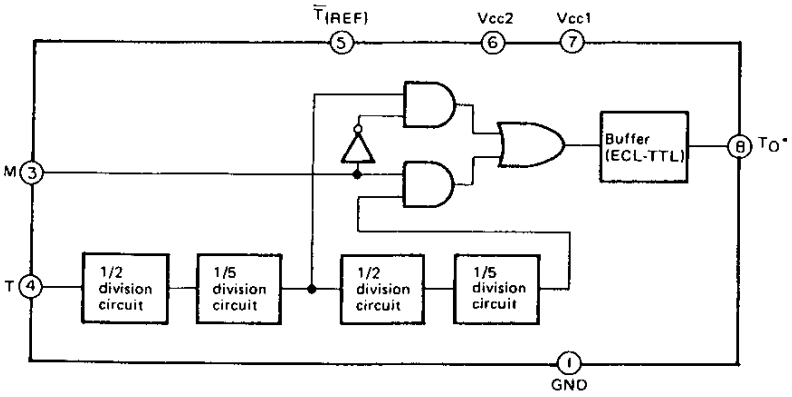
M	"L"	"H"
Division ratio	1/20	1/100

M54460L : Divider (Control unit IC5)

- **Terminal connection diagram**

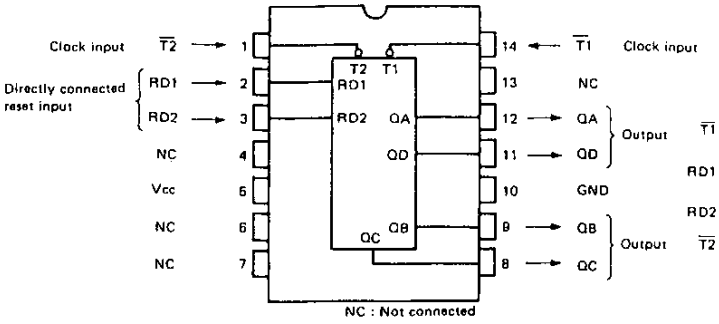


- **Block diagram**

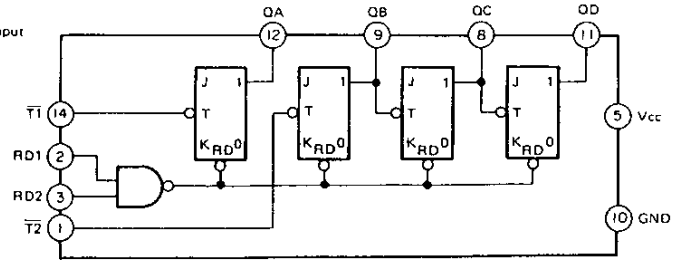


M74LS93P : Divider (Control unit IC8)

- **Terminal connection diagram**



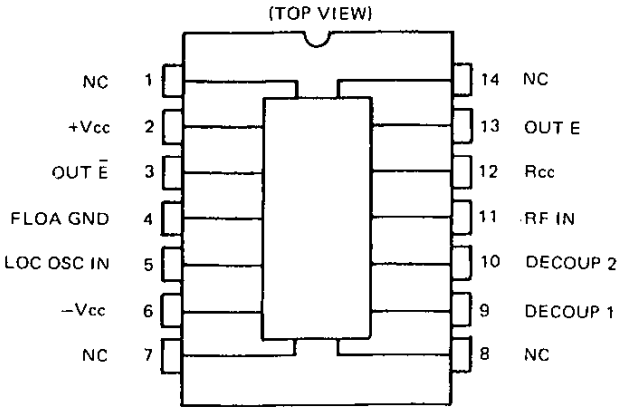
- **Logic circuit**



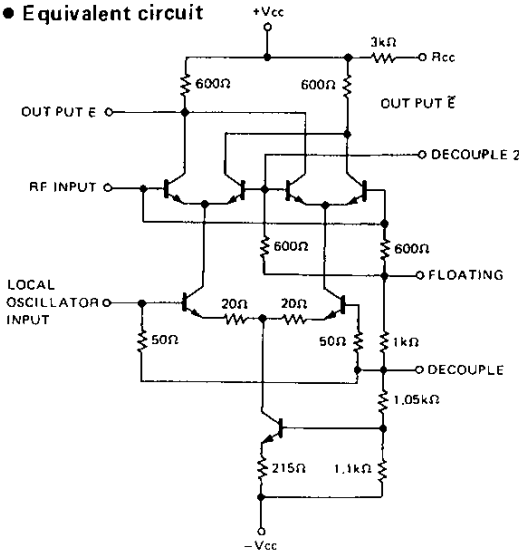
SEMICONDUCTOR DATA

SN76514N : Mixer (Control unit IC12)

- **Terminal connection diagram**

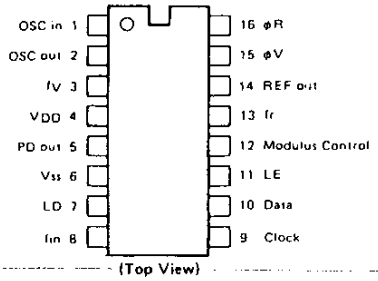


- **Equivalent circuit**



MB87006 : PLLIC (Control unit IC13)

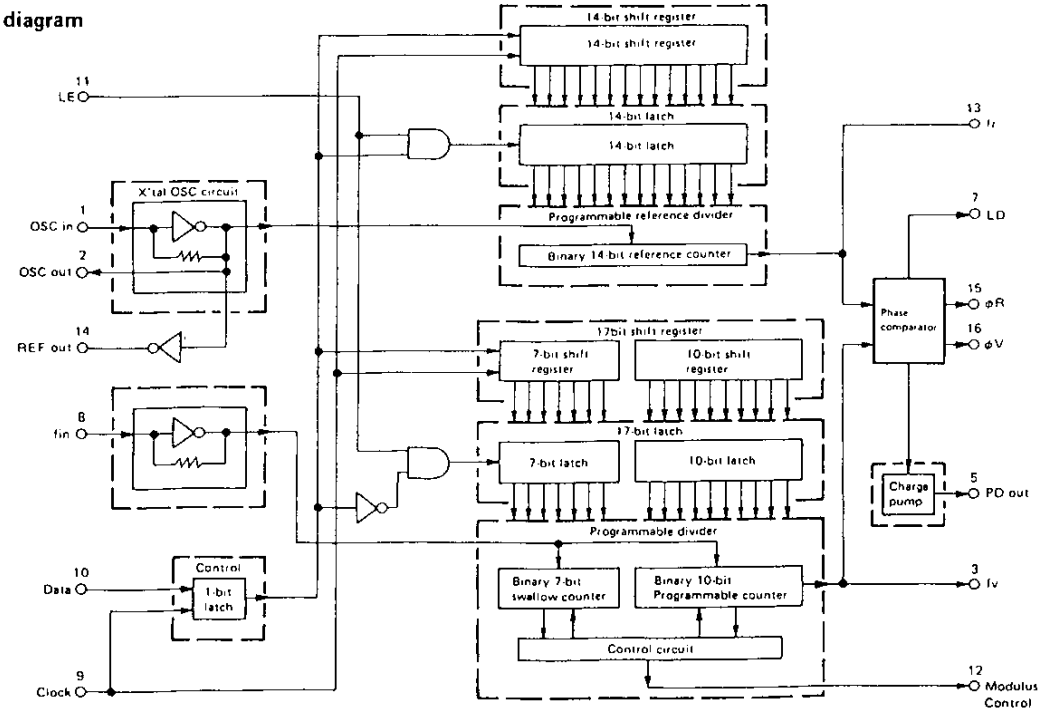
- **Terminal connection diagram**



- **Terminal function**

Terminal No.	I/O	Terminal name	Terminal No.	I/O	Terminal name
1	I	OSC in	9	I	Clock
2	O	OSC out	10	I	Data
3	O	fv	11	I	LE
4	–	V_{DD}	12	O	Modulus Control
5	O	PD out	13	O	fr
6	–	V_{SS}	14	O	REF out
7	O	LD	15	O	φV
8	I	fin	16	O	φR

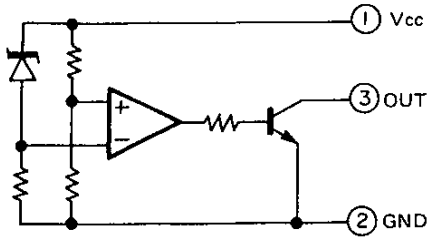
- **Block diagram**



SEMICONDUCTOR DATA

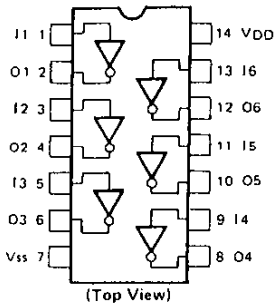
PST520D : System reset (Control unit IC15)

- **Equivalent circuit**



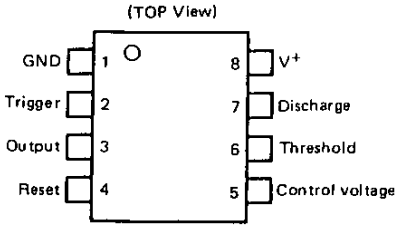
TC4069UBP : Inverter (Control unit IC16,25)

- **Block diagram**

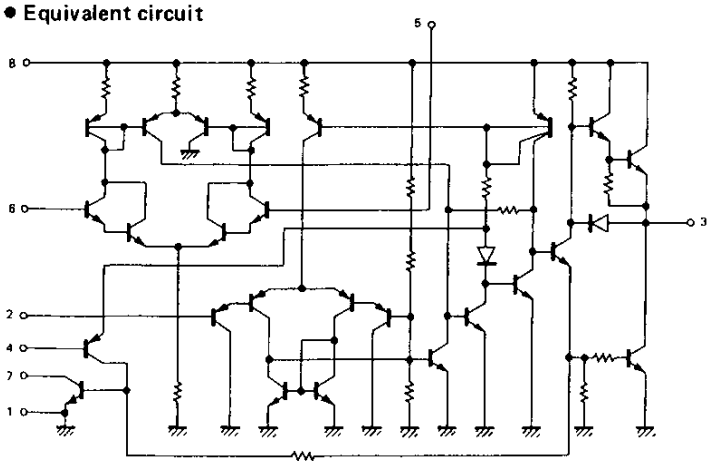


NE555C : System clock oscillator (Control unit IC17)

- **Terminal connection diagram**

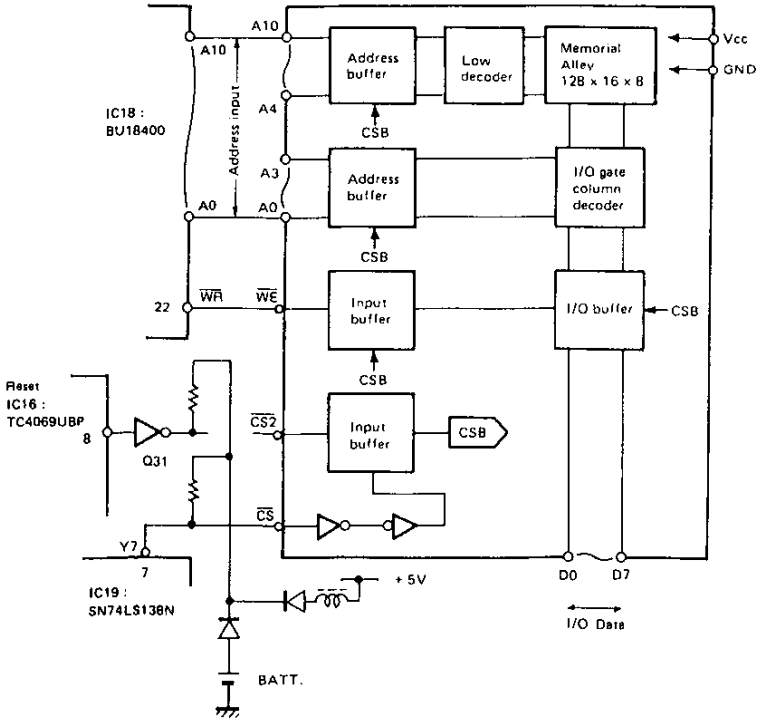


- **Equivalent circuit**



TC5518CPL-20 : Static RAM (Control unit IC20)

- **Block diagram**



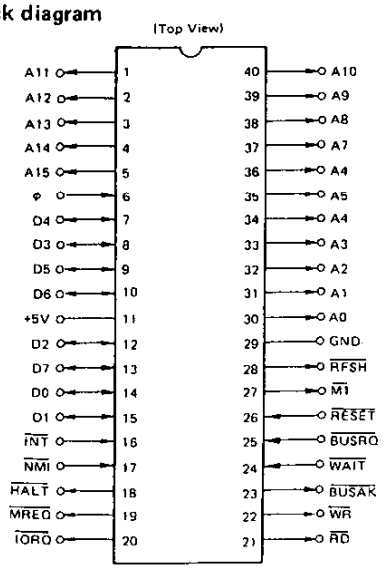
- **Terminal function**

Terminal name	Function
A0~A10	Address input
D0~D7	Data input/output
$\overline{CS}$	Chip select 1
$\overline{SC2}$	Chip select 2
$\overline{WE}$	Write enable
Vcc	Power supply (+ 5V)
GND	Ground

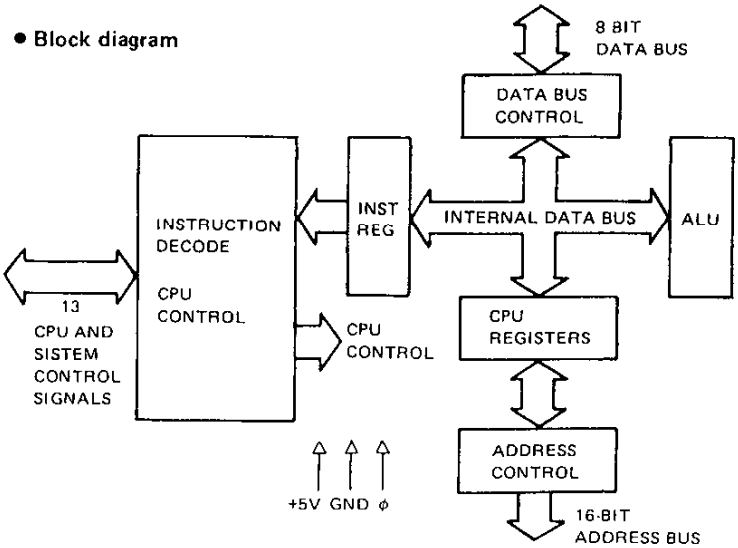
SEMICONDUCTOR DATA

BU18400A : CPU (Control unit IC18)

• **Block diagram**



• **Block diagram**



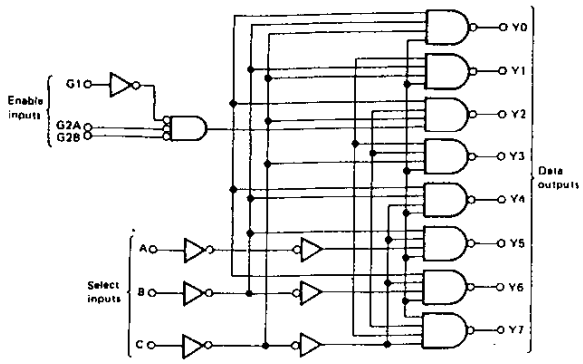
• **Terminal function**

Terminal (Signal) name	Input/Output	Terminal (Signal) function
A0 ~ A15 (Address Bus)	3-state output Active "H"	16-bit address bus. Outputs address of memory or I/O device No.. When memory is refreshed, refreshed address is output to seven bits at lower places.
D0 ~ D7 (Data Bus)	3-state Input/output Active "H"	8-bit data bus. Used to transfer data between memory or I/O device and CPU.
$\overline{M1}$ (Machin Cycle one)	Output Active "L"	Signal which indicates started machine cycle is OP code fetch cycle.
$\overline{MREQ}$ (Memory Request)	3-state output Active "L"	Signal which indicates address information necessary for reading and writing memory is output to address bus.
$\overline{IORQ}$ (Input/Output Request)	3-state output Active "L"	During M1 cycle This signal request outside devices to add interruption response vector to data bus when maskable interruption is acknowledged. Out of M1 cycle This signal indicates I/O device No. necessary for reading and writing I/O is output to the address bus.
$\overline{RD}$ (Read)	3-state output Active "L"	Signal which indicates data is being input in data bus. Memory or I/O device sends data to the data bus, synchronizing with this signal
$\overline{WR}$ (Write)	3-state output Active "L"	Signal which indicates data is being output by data bus. Data to be sent to memory or I/O device is supplied to data bus, synchronizing with this signal.
$\overline{RFSH}$ (Refresh)	Output Active "L"	Signal which indicates refreshed address for dynamic RAM is output to seven bits at lower places of address during M1 cycle. Dynamic RAM reads refreshed address by using $\overline{MREQ}$ signal output at the same time as $\overline{RFSH}$ signal.
$\overline{HALT}$ (Halt State)	Output Active "L"	Signal which indicates HALT command is executed and CPU is set under HALT condition. When returning from HALT condition, any one of INT, $\overline{NM1}$ or $\overline{RESET}$ signals is necessary. CPU continues to refresh memory executing NOP command during HALT.
WAIT (Wait)	Input Active "L"	While this signal is active, CPU continues to wait. If this signal is used, low-speed memory or I/O device can be directly connected to CPU. While CPU is waiting, memory is not refreshed.
$\overline{INT}$ (Interrupt Request)	Input Active "L"	Input terminal for interruption request signal. If this signal becomes active while interruption is permitted, CPU starts interruption program after finishing command being executed.
$\overline{NMI}$ (Non Maskable Interrupt)	Input Negative edge trigger	Input terminal for nonmaskable interruption request signal. If this signal becomes active, CPU jumps to address 0066 (16) after finishing command being executed, regardless of permission of interruption. Priority higher than $\overline{INT}$ signal is given to $\overline{NM1}$ signal.
$\overline{RESET}$ (Reset)	Input Active "L"	If this signal becomes active, CPU is reset.
$\overline{BUSRQ}$ (Bus Request)	Input Active "L"	If this signal becomes active, CPU heighten impedance of address bus (A0 ~ A15), data bus (D0 ~ D7) and 3-state system control terminals ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$). Thus, other devices can use above external buses. Priority higher than $\overline{NM1}$ signal is given to $\overline{BUSRQ}$ signal.
$\overline{BUSAK}$ (Bus Acknowledge)	Output Active "L"	Signal which indicates CPU has received $\overline{BUSRQ}$ signal and heightened impedance of address bus, data bus and 3-state system control terminal.
φ (Clock)	Input	+5V single-phase clock input terminal.

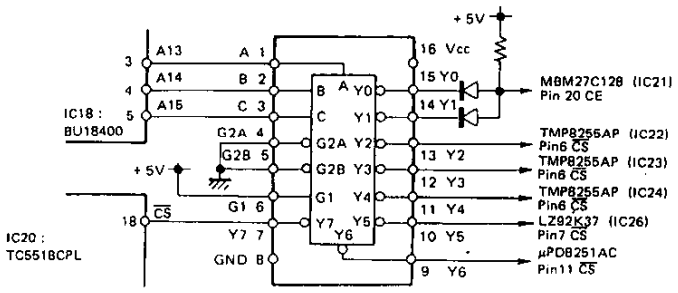
SEMICONDUCTOR DATA

SN74LS138N : Address decoder (Control unit IC19)

- Logic circuit



- Block diagram



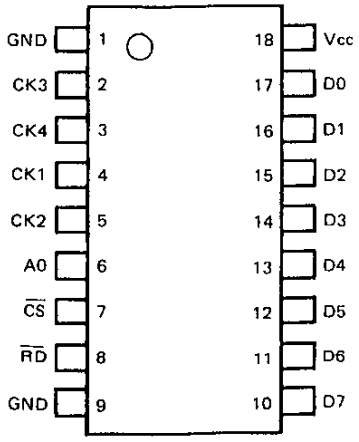
- Truth table

INPUT					OUTPUT							
Enable		Select										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : G2 = G2A + G2B
Note 2 : H : High level
L : Low level
X : Either "H" or "L"

LZ92K37 : Counter (Control unit IC26)

- Terminal connection diagram



- Terminal function

Pin No.	I/O	Signal name	Pin No.	I/O	Signal name
1	–	GND	10	TO	D7
2	Icu	CK3	11	TO	D6
3	Icu	CK4	12	TO	D5
4	Icu	CK1	13	TO	D4
5	Icu	CK2	14	TO	D3
6	Ic	A0	15	TO	D2
7	Ic	CS	16	TO	D1
8	Ic	RD	17	TO	D0
9	–	GND	18	–	Vcc

Ic : C-MOS level input buffer
Icu : Input buffer with C-MOS level pull-up resistance
TO : Tristate output buffer

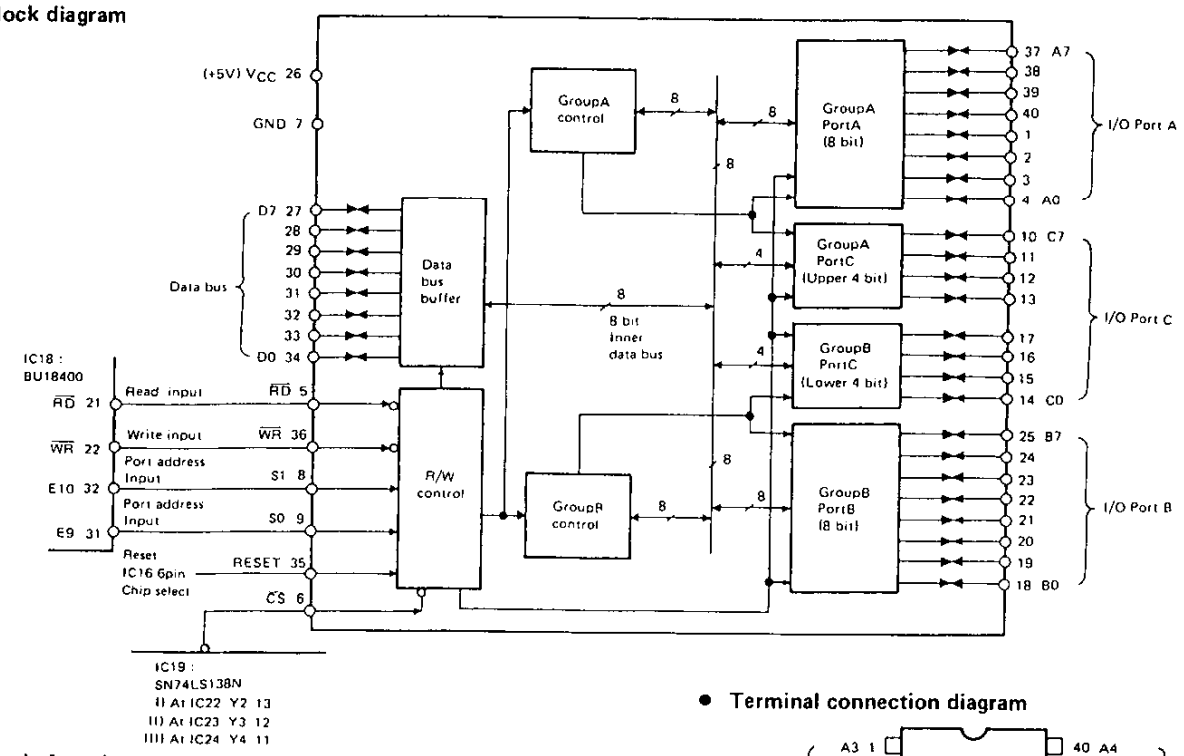
- Terminal function

Terminal name	Terminal function
CK1, 2	Rotary encoder pulse input
CK3, 4	Rotary encoder pulse input
A0	Output data selection input, 0 = CK1, 2 1 = CK3, 4
CS	Chip select input
RD	Read enable input
D0 ~ D7	Data bus output

SEMICONDUCTOR DATA

TMP8255AP-5 : I/O Port (Control unit IC22~24)

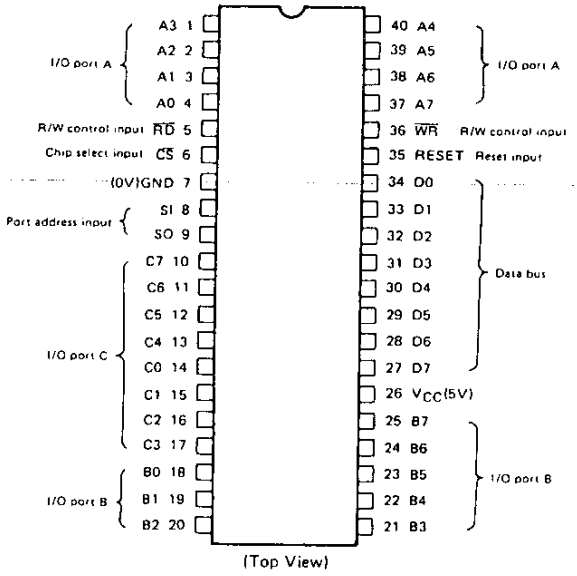
- **Block diagram**



- **Basic function**

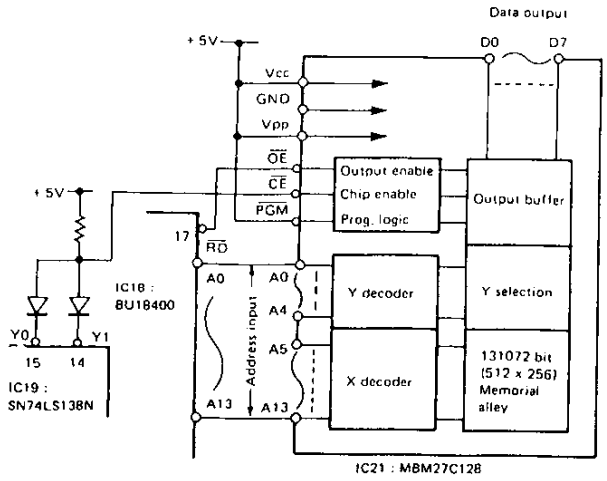
SI	SO	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Function
L	L	L	L	H	Data bus ← Port A
L	H	L	L	H	Data bus ← Port B
H	L	L	L	H	Data bus ← Port C
L	L	L	H	L	Port A ← Data bus
L	H	L	H	L	Port B ← Data bus
H	L	L	H	L	Port C ← Data bus
H	H	L	H	L	Control register ← Data bus
–	–	H	–	–	Data bus is in the high-impedance state.
H	H	L	L	H	Prohibit assortment

- **Terminal connection diagram**



MBM27C128-25JAJ2 : ROM (Control unit IC21)

- **Block diagram**



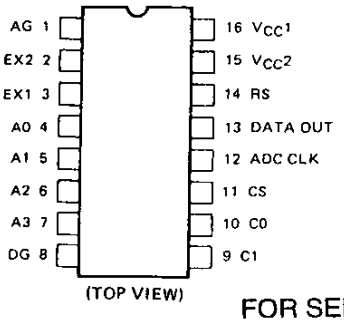
- **Terminal function**

Terminal name	Function
A0~A13	Address input
D0~D7	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{PGM}$	Program input
Vcc	Power supply
Vpp	Program power supply
GND	Ground

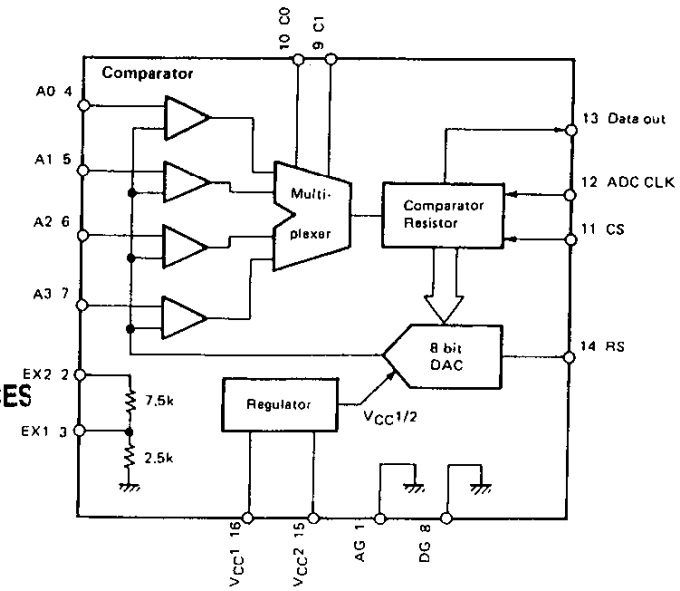
SEMICONDUCTOR DATA

MB4052 : A/D Converter (Control unit IC27)

• **Terminal connection diagram**



• **Block diagram**



• **I/O signal pin function**

Pin No.	Pin name	Symbol	Function
1	Analog ground	AG	Ground terminal
2	Range expander input	EX2	Analog input pin for expanding the range.
3	Range expander output	EX1	Analog output pin for expanding the range. Connect to any pin from A0 to A3. By using EX1, EX2, the range is expanded to the X 4 range.
4~7	Analog entrance	A0~A3	4-ch analog input pin. Channel 1 is selected by channel select input C0 to C1.
8	Digital ground	DG	Ground terminal
9	Channel select input	C0	The input pin to designate the analog input channel for A/D converter. This signal is latched at the trailling edge of CS.
10		C1	
11	Chip select input	CS	This is the chip select input pin. When CS is inverted from "1" to "0", A/D converting starts and data output is enabled. After A/D converting is over or when an interrupt is required, set the CS back to "1".
12	A/D conversion clock	ADC CLK	This is the clock input pin for A/D conversion input to the comparator register sequentially. Conversion speed is determined by the clock speed. In the case of 8-bit, approx. 10 clocks will be needed. However, it is not necessary that the clock period be fixed.
13	Data output	DATA OUT	This is the open collector to output the result of A/D conversion. The data is output in the order of the start bit, most significant bit, 2nd significant bit, . . . , least significant bit, and the stop bit, synchronized with ADCCLK.
14	Range select input	RS	This is the input pin for selecting the voltage range of analog input. The VFS = VCC1/8 range is selected at "0", and the range of FVS = VCC1/2 is selected at "1". During conversion, hold this pin to "0" or "1".
15 16	Power supply pin 2 Power supply pin 1	VCC2 VCC1	When driving with 3.5V to 6.0V of power, connect VCC1 and VCC2 to each other, and apply the power voltage to them. When driving 8 to 18V of power, apply the power voltage to VCC2. At this time, the 5V stabilized voltage is output to VCC1, and approx. 10mA current can be supplied externally to the IC. When either 3.5~6.0V or 8~18V power is used, VCC1 is the reference voltage for A/D conversion.

• **Channel select**

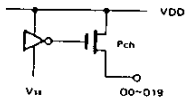
C1	C0	Selected Ch.
0	0	A0
0	1	A1
1	0	A2
1	1	A3

• **Range select**

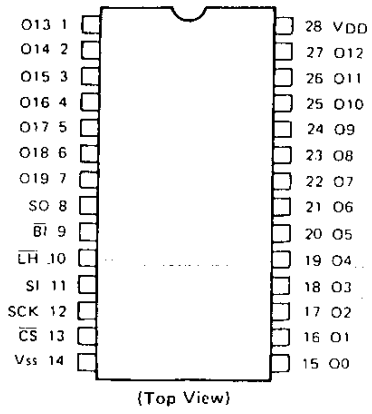
RS	Conversion voltage range
0	$0 \sim \frac{Vcc1}{8}$
1	$0 \sim \frac{Vcc1}{2}$

μPD6300C : Fluorescent display tube driver (Display unit IC1)

- Terminal function

Terminal No.	Symbol	Terminal name	I/O	Function
1~7	O13~O19	FIP segment driver	O	High dielectric-strength (40V) output in the Pch open. Corresponds to the output of O13~O19.
8	SO	Serial data output pin	O	Output serial data the trailing edge of SCK, when the n-number of μPD6300Cs are connected in series, this can be connected to the SI of the following stage.
9	$\overline{BI}$	Blanking pin	I	This input can turn off all indicator or displays, and can dim them by applying a random duty pulse from outside. Active low.
10	$\overline{LH}$	Latch pin	I	Transmits the connects of the serial shift register to the buffer register at low level, to latch the connects at the rising time. Active rising (leading) edge.
11	SI	Serial data input pin	I	This is the data input pin. Inputs data to the shift register at the rising edge of SCK.
12	SCK	Serial clock input pin	I	Reads out the SI data to the shift register at the rising edge of SCK. Outputs data from SO at the trailing edge of SCK.
13	$\overline{CS}$	Chip select pin	I	When CS is high, this inhibits SCK and $\overline{LH}$, and when CS is low, activates SCK and $\overline{LH}$.
14	Vss	GND	–	Connect to the GND terminal of the system.
15~27	O0~O12	FIP segment driver	O	Pch open-drain system, high dielectric-strength output. Corresponds to the output of O0~O12. 
28	VDD	Power supply pin	–	5V ± 10%

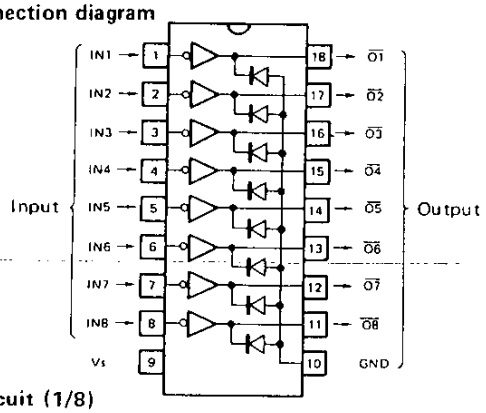
- Terminal connection diagram



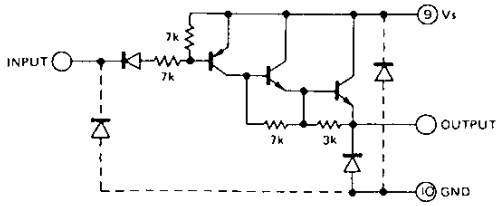
(Top View)

M54581P : Band data driver (Signal unit IC1)

- Terminal connection diagram

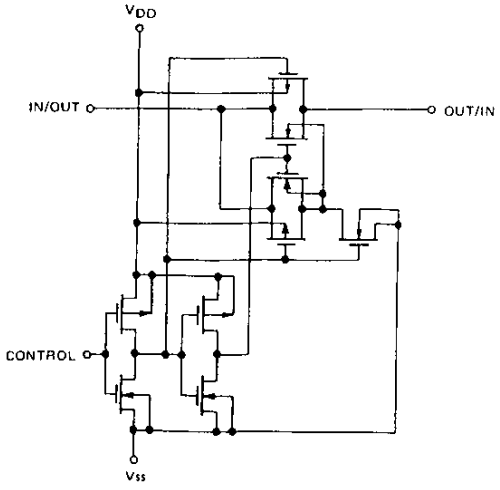


- Equivalent circuit (1/8)

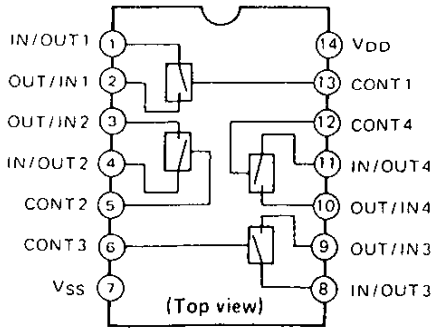


TC4066BP : Switch (Signal unit IC7~10)

- Equivalent circuit (1/4)



- Terminal connection diagram



(Top view)